RTAX-S/SL RadTolerant FPGAs

Radiation Performance

- SEU-Hardened Registers Eliminate the Need for Triple-Module Redundancy (TMR)
  - Immune to Single-Event Upsets (SEU) to LET_{TH} > 37 MeV-cm^2/mg
  - SEU Rate < 10^{-10} Errors/Bit-Day in Worst-Case Geosynchronous Orbit
- Expected SRAM Upset Rate of <10^{-10} Errors/Bit-Day with Use of Error Detection and Correction (EDAC) IP (included) with Integrated SRAM Scrubber
  - Single-Bit Correction, Double-Bit Detection
  - Variable-Rate Background Refreshing
- Total Ionizing Dose Up to 300 krad (Si, Functional)
- Single-Event Latch-Up Immunity (SEL) to LET_{TH} > 117 MeV-cm^2/mg
- TM1019 Test Data Available
- Single Event Transient (SET) – No Anomalies up to 150 MHz

Processing Flows

- B-Flow – MIL-STD-883B
- E-Flow – Actel Extended Flow
- EV-Flow – Class V Equivalent Flow Processing Consistent with MIL-PRF 38535

Prototyping Options

- Commercial Axcelerator Devices for Functional Verification
- RTAX-S PROTO Devices with Same Functional and Timing Characteristics as Flight Unit in a Non-Hermetic Package
- Low Priced Reprogrammable ProASIC®3 Option for Functional Verification

RTAX-SL Low Power Option

- Offers Approximately Half the Standby Current of the Standard RTAX-S Device at Worst-Case Conditions

Leading-Edge Performance

- High-Performance Embedded FIFOs
- 350+ MHz System Performance
- 500+ MHz Internal Performance
- 700 Mb/s LVDS Capable I/Os

Specifications

- Up to 4 Million Equivalent System Gates or 500 k Equivalent ASIC Gates
- Up to 20,160 SEU-Hardened Flip-Flops
- Up to 840 I/Os
- Up to 540 kbits Embedded SRAM
- Manufactured on Advanced 0.15 µm CMOS Antifuse Process Technology, 7 Layers of Metal
- Electrostatic Discharge (ESD) is 2,000 V (HBM MIL-STD-883, TM3015)

Features

- Single-Chip, Nonvolatile Solution
- 1.5 V Core Voltage for Low Power
- Flexible, Multi-Standard I/Os:
  - 1.5 V, 1.8 V, 2.5 V, 3.3 V Mixed Voltage Operation
  - Bank-Selectable I/Os – 8 Banks per Chip
  - Single-Ended I/O Standards: LVTTL, LVCMOS, 3.3 V PCI
  - JTAG Boundary Scan Testing (as per IEEE 1149.1)
  - Differential I/O Standards: LVPECL and LVDS
  - Voltage-Referenced I/O Standards: GTL+, HSTL Class 1, SSTL2 Class 1 and 2, SSTL3 Class 1 and 2
  - Hot-Swap Compliant with Cold-Sparing Support (Except PCI)
- Embedded Memory with Variable Aspect Ratio and Organizations:
  - Independent, Width-Configurable Read and Write Ports
  - Programmable Embedded FIFO Control Logic
  - ROM Emulation Capability
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Debug Capability

Table 1 • **RTAX-S/SL Family Product Profile**

Device	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
Capacity				
Equivalent System Gates	250,000	1,000,000	2,000,000	4,000,000
ASIC Gates	30,000	125,000	250,000	500,000
Modules				
Register (R-cells)	1,408	6,048	10,752	20,160
Combinatorial (C-cells)	2,816	12,096	21,504	40,320
Flip-Flops (maximum)	2,816	12,096	21,504	40,320
Embedded RAM/FIFO (without EDAC)				
Core RAM Blocks	12	36	64	120
Core RAM Bits (K = 1,024)	54 k	162 k	288 k	540 k
Clocks (segmentable)				
Hardwired	4	4	4	4
Routed	4	4	4	4
I/Os				
I/O Banks	8	8	8	8
User I/Os (maximum)	198	418	684	840
I/O Registers	744	1,548	2,052	2,520
Package				
CCGA/LGA	624	624	624, 1152	1272
CQFP	208, 352	352	256, 352	352

Ordering Information

RTAX2000S/SL – 1 CGS 624 B

- Application
  - B = MIL-STD 883 Class B
  - E = E-Flow (Actel Space-Level Flow)
  - EV = Class V Equivalent Flow Processing Consistent with MIL-PRF 38535
- Package Lead Count
- Package Type
  - CQ = Ceramic Quad Flat Pack
  - CG = Ceramic Column Grid Array
  - LG = Land Grid Array
  - S = Six Sigma Column
- Speed Grade
  - Blank = Standard Speed
  - 1 = Approximately 15% Faster than Standard (applies to RTAX250S/SL, RTAX1000S/SL. RTAX2000S/SL)
  - 1 = Approximately 10% Faster than Standard (applies to RTAX4000S/SL)
- Part Number
  - S = Standard Family
  - SL = Low-Power Option
  - RTAX250S/SL = 250,000 Equivalent System Gates
  - RTAX1000S/SL = 1,000,000 Equivalent System Gates
  - RTAX2000S/SL = 2,000,000 Equivalent System Gates
  - RTAX4000S/SL = 4,000,000 Equivalent System Gates

Note: PROTO refers to the RTAX-S/SL Prototype Units. All CCGA PROTO units will be offered with the Six Sigma Column.

Temperature Grade Offerings

Package	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
CQ208	B, E, EV	–	–	–
CQ256	–	–	B, E, EV	–
CQ352	B, E, EV	B, E, EV	B, E, EV	B, E, EV
CG624/LG624	B, E, EV	B, E, EV	B, E, EV	–
CG1152/LG1152	–	–	B, E, EV	–
CG1272/LG1272	–	–	–	B, E, EV

Note: *B = MIL-STD-883 Class B*
E = E-Flow (Actel Space-Level Flow)
EV = Actel "V" Equivalent Flow (Class V processing consistent with MIL-PRF 38535)

Speed Grade and Temperature Grade Matrix

	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
STD	✓	✓	✓	✓
-1	✓	✓	✓	✓

Notes:

1. *Data applies to B,E,EV flow devices.*
2. *Contact your Actel representative for availability.*

Device Resources

	User I/Os (Including Clock Buffers)			
Device	**RTAX250S/SL**	**RTAX1000S/SL**	**RTAX2000S/SL**	**RTAX4000S/SL**
CQ208	115	–	–	–
CQ256	–	–	136	–
CQ352	198	198	198	166
CG624/LG624	232	418	418	–
CG1152/LG1152	–	–	684	–
CG1272/LG1272	–	–	–	840

Note: *CQFP = Ceramic Quad Flat Pack and CCGA = Ceramic Column Grid Array, LGA = Land Grid Array*

I/Os per Package

Package	Device	Single-Ended	Differential Pair	Pair	Total I/Os
CQ208	RTAX250S	7	41	13	115
CQ256	RTAX2000S	4	66	0	136
CQ352	RTAX250S	2	98	0	198
	RTAX1000S	2	98	0	198
	RTAX2000S	2	98	0	198
	RTAX4000S	4	81	0	166
CG624	RTAX250S	0	124	0	248
	RTAX1000S	68	170	5	418
	RTAX2000S	52	178	5	418
CG1152	RTAX2000S	0	342	0	684
CG1272	RTAX4000S	0	420	0	840

Actel MIL-STD-883 Class B Product Flow

Table 2 • **Actel MIL-STD-883 Class B Product Flow for RTAX-S/SL[1, 2]**

Step	Screen	Method	Requirement
1	Internal Visual	2010, Condition B	100%
2	Serialization		100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	2001, Y1 Orientation Only Condition B for CQ352, LG624, LG1152 Condition D for CQ208 Condition A[3] for LG1272, CQ352	100%
5	Particle Impact Noise Detection	2020, Condition A	100%
6	Seal (Fine & Gross Leak Test)	1014	100%
7	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
8	Dynamic Burn-In	1015, Condition D, 160 hours at 125°C or 80 hours at 150°C minimum	100%
9	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
10	Percent Defective Allowable (PDA) Calculation	5%	All Lots
11	Final Electrical Test[2] a. Static Tests (1) 25°C (2) –55°C and +125°C b. Functional Tests (1) 25°C (2) –55°C and +125°C c. Switching Tests at 25°C	In accordance with applicable Actel device specification, which includes a, b, and c: 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b 5005, Table 1, Subgroup 9	100%
12	External Visual	2009	100%

Notes:

1. *For CCGA devices, all Assembly, Screening, and TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.*
2. *RTAX-S and RTAX-SL devices have the same silicon and are distinguished by screening the I_{CCA} current limits at 125°C final electrical test.*
3. *Condition A applies to RTAX4000S/SL packages only.*

Actel Extended Flow

Table 3 • **Actel Extended Flow for RTAX-S/SL[1, 2, 3, 4]**

Step	Screen	Method	Requirement
1	Destructive Bond Pull[5]	2011, Condition D	Extended Sample
2	Internal Visual	2010, Condition A	100%
3	Serialization		100%
4	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
5	Constant Acceleration	2001, Y1 Orientation Only Condition B for CQ352, LG624, LG1152 Condition D for CQ208 Condition A[5] for LG1272, CQ352	
6	Particle Impact Noise Detection	2020, Condition A	100%
7	Radiographic (X-Ray)	2012, One View (Y1 Orientation) Only	100%
8	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125°C or 120 hours at 150°C minimum	100%
10	Interim (Post-Dynamic-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
11	Static Burn-In	1015, Condition C, 72 hours at 150°C or 144 hours at 125°C minimum	100%
12	Interim (Post-Static-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
13	Percent Defective Allowable (PDA) Calculation	5% Overall, 3% Functional Parameters at 25°C	All Lots
14	Final Electrical Test[4] a. Static Tests (1) 25°C (2) –55°C and +125°C b. Functional Tests (1) 25°C (2) –55°C and +125°C c. Switching Tests at 25°C	In accordance with applicable Actel device specification, which includes a, b, and c: 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b 5005, Table 1, Subgroup 9	100%
15	Seal (Fine & Gross Leak Test)	1014	100%
16	External Visual	2009	100%

Notes:

1. *Actel offers Extended Flow for users requiring additional screening beyond MIL-STD-833, Class B requirement. Actel is offering this Extended Flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S.*
2. *The Quality Conformance Inspection (QCI) for Extended Flow devices still comply to MIL-STD-833, Class B requirement.*
3. *For CCGA devices, all Assembly/Screening/TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.*
4. *RTAX-S and RTAX-SL devices have the same silicon and are distinguished by screening the I_{CCA} current limits at 125°C final electrical test.*
5. *Condition A applies to RTAX4000S/SL packages only.*
6. *Requirement for 100% nondestructive bond pull per Method 2003 is substituted by an extensive destructive bond pull to Method 2011 Condition D on an extended sample basis.*

Actel "EV" Flow (Class V Flow Equivalent Processing)

Table 4 • **Actel "EV" Flow (Class V Equivalent Flow Processing) for RTAX-S/SL[1, 2, 3]**

Step	Screen	Method	Requirement
1	Destructive Bond Pull[4]	2011, Condition D	Extended Sample
2	Internal Visual	2010, Condition A	100%
3	Serialization		100%
4	Temperature Cycling	1010, Condition C, 50 cycles minimum	100%
5	Constant Acceleration	2001, Y1 Orientation Only Condition B for CQ352, LG624, LG1152 Condition D for CQ208 Condition A[5] for LG1272, CQ352	100%
6	Particle Impact Noise Detection	2020, Condition A	100%
7	Radiographic (X-Ray)	2012, One View (Y1 Orientation) Only	100%
8	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125°C or 120 hours at 150°C minimum	100%
10	Interim (Post-Dynamic-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
11	Static Burn-In	1015, Condition C, 72 hours at 150°C or 144 hours at 125°C minimum	100%
12	Interim (Post-Static-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
13	Percent Defective Allowable (PDA) Calculation	5% Overall, 3% Functional Parameters at 25°C	All Lots
14	Final Electrical Test[3] a. Static Tests (1) 25°C (2) –55°C and +125°C b. Functional Tests (1) 25°C (2) –55°C and +125°C c. Switching Tests at 25°C	In accordance with applicable Actel device specification, which includes a, b, and c: 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b 5005, Table 1, Subgroup 9	100%
15	Seal (Fine & Gross Leak Test)	1014	100%
16	External Visual	2009	100%
17	Wafer Lot Specific Life Test (Group C)	MIL-PRF-38535, Appendix B, sec. B.4.2.c	All Wafer Lots

Notes:

1. *Actel offers "EV" flow for users requiring full compliance to MIL-PRF-38535 class V requirement. The "EV" process flow is expanded from the existing E-flow requirement (it still meets the full SMD requirement for current E-flow devices) with the intention to be in full compliance to MIL-PRF-38535 Table IA and Appendix B requirement, but without the official class V certification from DSCC.*
2. *For CCGA devices, all Assembly/Screening/TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.*
3. *RTAX-S and RTAX-SL devices have the same silicon and are distinguished by screening the I_{CCA} current limits at 125°C final electrical test.*
4. *Condition A applies to RTAX4000S/SL packages only.*
5. *Requirement for 100% nondestructive bond pull per Method 2003 is substituted by an extensive destructive bond pull to Method 2011 Condition D on an extended sample basis.*

Table of Contents

General Description

RTAX-S/SL offers high performance at densities of up to four million equivalent system gates for space-based applications. Based upon the Actel commercial Axcelerator® family, RTAX-S/SL has several system-level features such as embedded SRAM (with built-in FIFO control logic), segmentable clocks, chip-wide highway routing, and carry logic.

Featuring SEU-hardened flip-flops that offer the benefits of user-implemented Triple Module Redundancy (TMR) without the associated overhead, the RTAX-S/SL family is the second generation Actel product offering for space applications. The RTAX-S/SL devices are manufactured using a 0.15 µm technology at a UMC facility in Taiwan. These devices offer levels of radiation survivability far in excess of typical CMOS devices.

Device Architecture

Actel RTAX-S/SL architecture, derived from the highly-successful A54SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1-1). Unlike traditional FPGAs, the entire floor of the RTAX-S/SL device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

Programmable Interconnect Element

The RTAX-S/SL family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 1-2 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the RTAX-S family abundant routing resources.

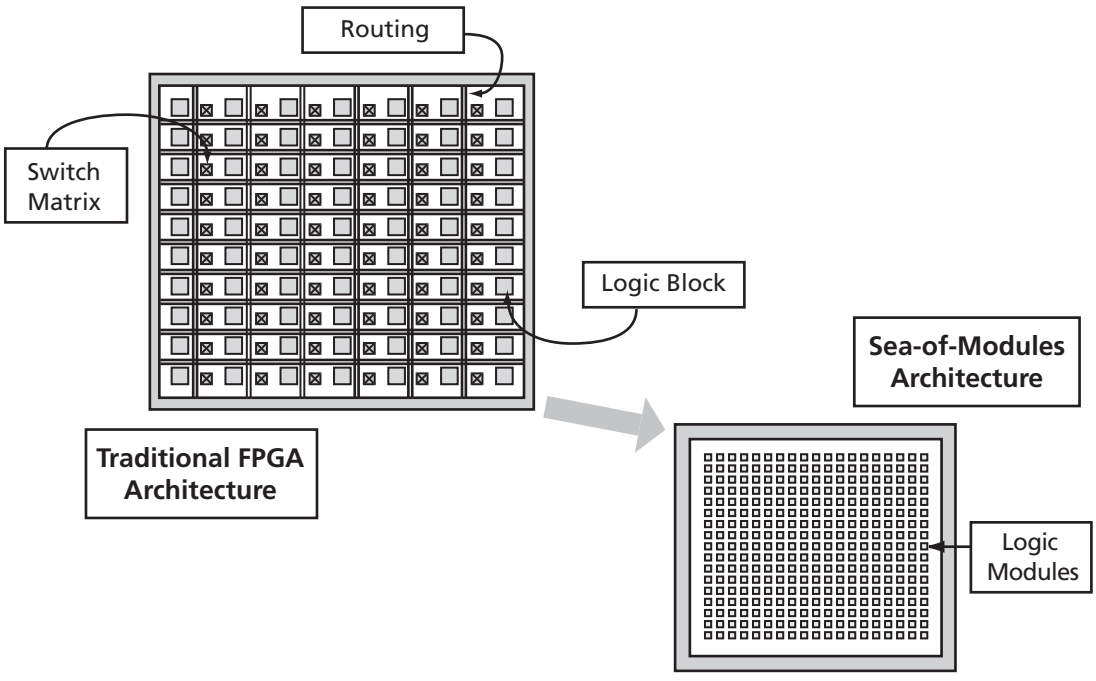


Figure 1-1 • **Sea-of-Modules Comparison**

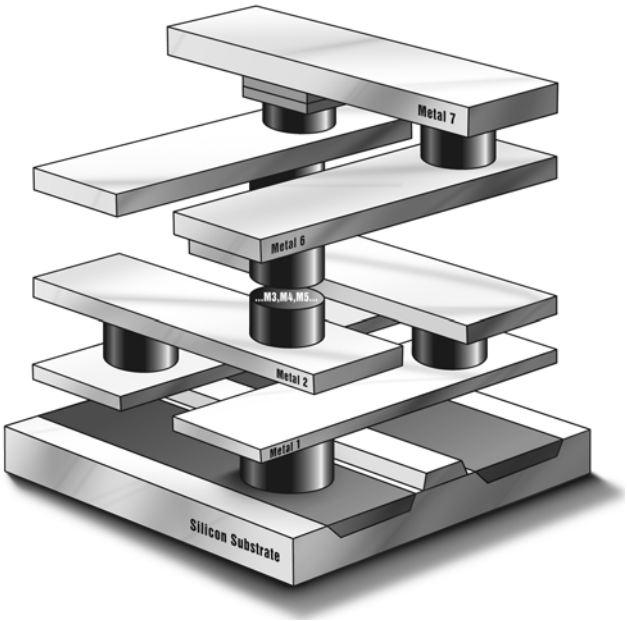


Figure 1-2 • **RTAX-S/SL Family Interconnect Elements**

The very nature of Actel's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock® technology). Cloning is impossible (even if the security fuse is left unprogrammed) as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see "Security" on page 2-101).

Actel's RTAX-S/SL family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The RTAX-S/SL C-cell can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3 on page 1-3). The C-cell contains carry logic for even more efficient implementation of arithmetic functions. With its small size, the C-cell structure is extremely synthesis-friendly, simplifying the overall design as well as reducing design time.

While each SEU-hardened R-cell appears as a single D-Type flip-flop to the user, each is implemented in silicon using triple redundancy to achieve a LET threshold of greater than 60 MeV-mg/cm^2. Each TMR R-cell consist of three master-slave latch pairs, each with asynchronous self-correcting feedback paths. The output of each latch on the master or slave side votes with the outputs of the other two latches on that side. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents that change from feeding back and permanently latching. Care was also taken in the layout to ensure that a single ion strike could not affect more than one latch (see "R-Cell" on page 2-66 for more details).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3 on page 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

Two C-cells, a single R-cell, and two Transmit (TX) and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (Figure 1-4 on page 1-3). Each SuperCluster also contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

The logic modules within the SuperCluster are arranged so that two combinatorial modules are side-by-side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance (Figure 1-5 on page 1-3).

The RTAX-S/SL architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

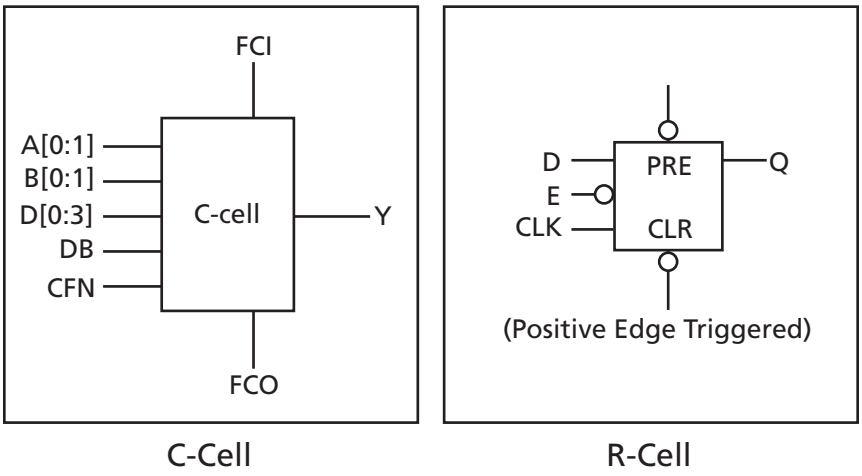


Figure 1-3 • **RTAX-S/SL C-Cell and R-Cell**

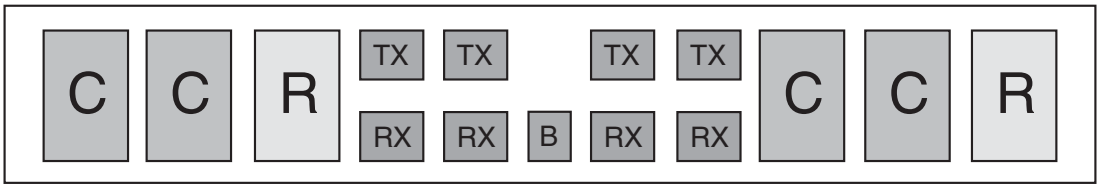


Figure 1-4 • **RTAX-S/SL SuperCluster**

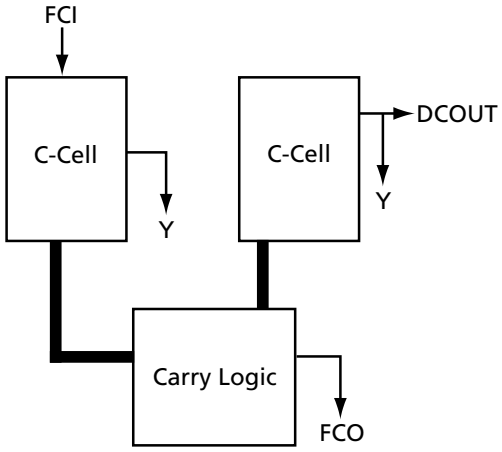


Figure 1-5 • **RTAX-S/SL Two-Bit Carry Logic**

At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. For example, the RTAX1000S/SL is composed of a 3×3 array of nine core tiles. Surrounding the array of core tiles are blocks of I/O Clusters and the I/O bank ring (Table 1-1).

Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and three SRAM blocks for the RTAX250S/SL). The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6).

Table 1-1 • **Number of Core Tiles per Device**

Device	Number of Core Tiles
RTAX250S/SL	4 smaller tiles
RTAX1000S/SL	9 regular tiles
RTAX2000S/SL	16 regular tiles
RTAX4000S/SL	30 regular tiles

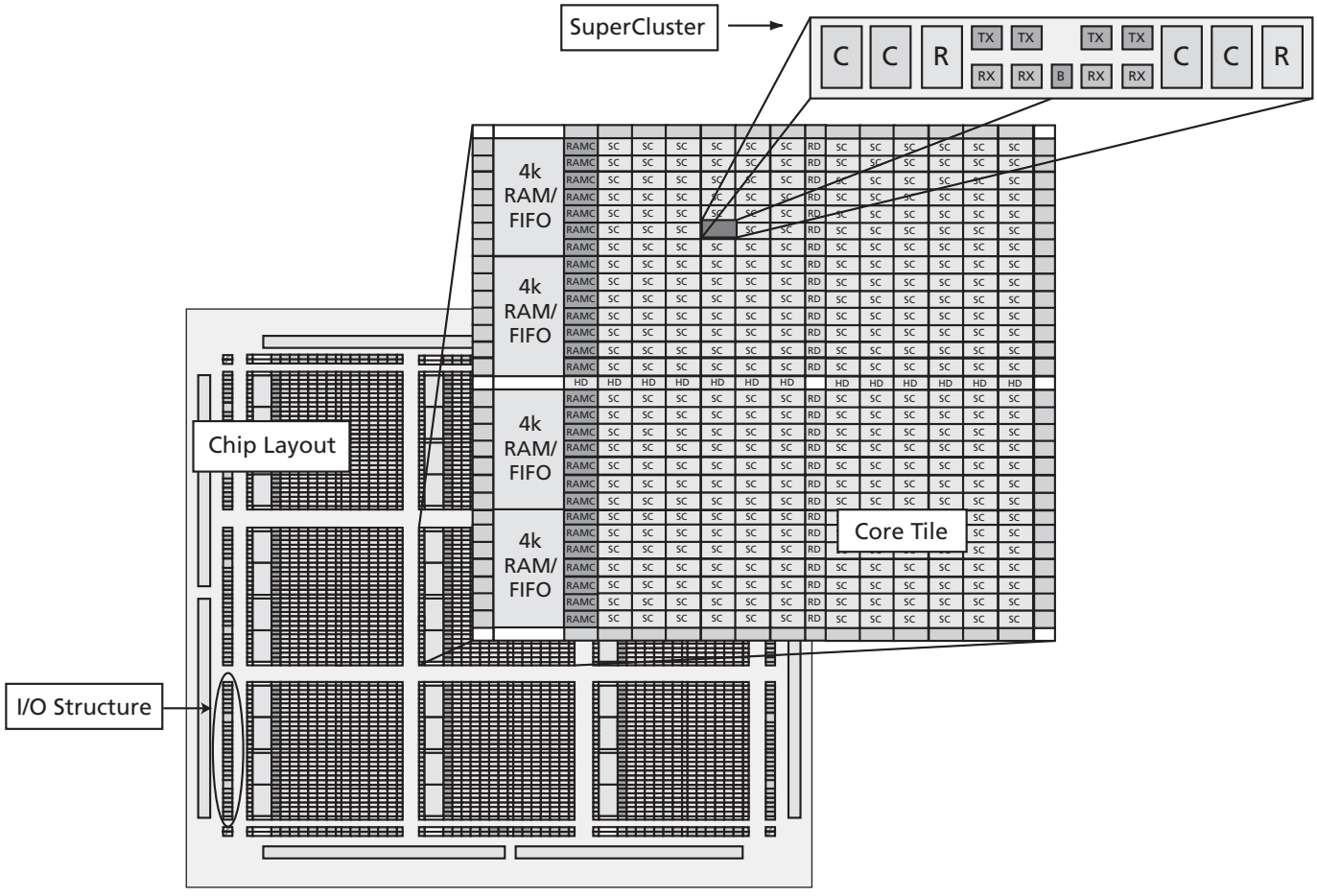


Figure 1-6 • **RTAX-S/SL Device Architecture (RTAX1000S/SL shown)**

Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

The FIFO control unit was not implemented with SEU-hardened registers. Designs requiring high SEU tolerance should implement the FIFO control unit from hardened core logic.

SRAM structures are inherently susceptible to upsets caused by high-energy particles encountered in space. High-energy particles can cause an SRAM cell to change state, resulting in the loss or corruption of a valuable data bit. Actel has enhanced the SEU tolerance of the embedded SRAM within RTAX-S/SL by employing the use of two upset-mitigation techniques:

- Actel has developed Error Detection and Correction (EDAC) IP for use with RTAX-S/SL. EDAC can be accomplished by the use of SmartGen-generated Error Correcting Codes (ECC) IP, which employs the use of shortened Hamming Codes
- A background memory-refresher, or scrubber circuitry, which has been embedded into the EDAC IP. The embedded scrubber circuitry periodically refreshes memory in the background to ensure that no data corruption occurs while the memory is not in use.

The use of EDAC IP combined with the embedded memory scrubber circuitry, gives the RTAX-S/SL an SEU radiation performance level of better than 10^{-10} errors/bit-day. See the application note *Using EDAC RAM for RadTolerant RTAX-S/SL FPGAs and Axcelerator FPGAs*.

I/O Logic

The RTAX-S/SL family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5 V, 1.8 V, 2.5 V, and 3.3 V. In all, RTAX-S/SL FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-12 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-6). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

By design, all user flip-flops in the RTAX-S FPGAs are immune to SEUs including the following three registers located in every I/O cell buffer: InReg, OutReg, and EnReg.

Routing

The RTAX-S/SL hierarchical routing structure ties the logic modules, the embedded memory blocks, and the I/O modules together (Figure 1-8 on page 1-6). At the lowest level, in and between SuperClusters, there are three local routing structures: FastConnect, DirectConnect, and CarryConnect routing. DirectConnects provide the highest performance routing inside the SuperClusters by connecting a C-cell to the adjacent R-cell. DirectConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

FastConnects provide high-performance, horizontal routing inside the SuperCluster and vertical routing to the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum routing delay of 0.4 ns.

CarryConnects are used for routing carry logic between adjacent SuperClusters. They connect the carry-logic FCO output of one C-cell pair to the carry-logic FCI input of the C-cell pair of the SuperCluster below. CarryConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

The next level contains the core tile routing. Over the SuperClusters within a core tile, both vertical and horizontal tracks run across rows or columns, respectively. At the chip level, vertical and horizontal tracks extend across the full length of the device, both north-to-south and east-to-west. These tracks are composed of highway routing that extend the entire length of the device (segmented at core tile boundaries) as well as segmented routing of varying lengths.

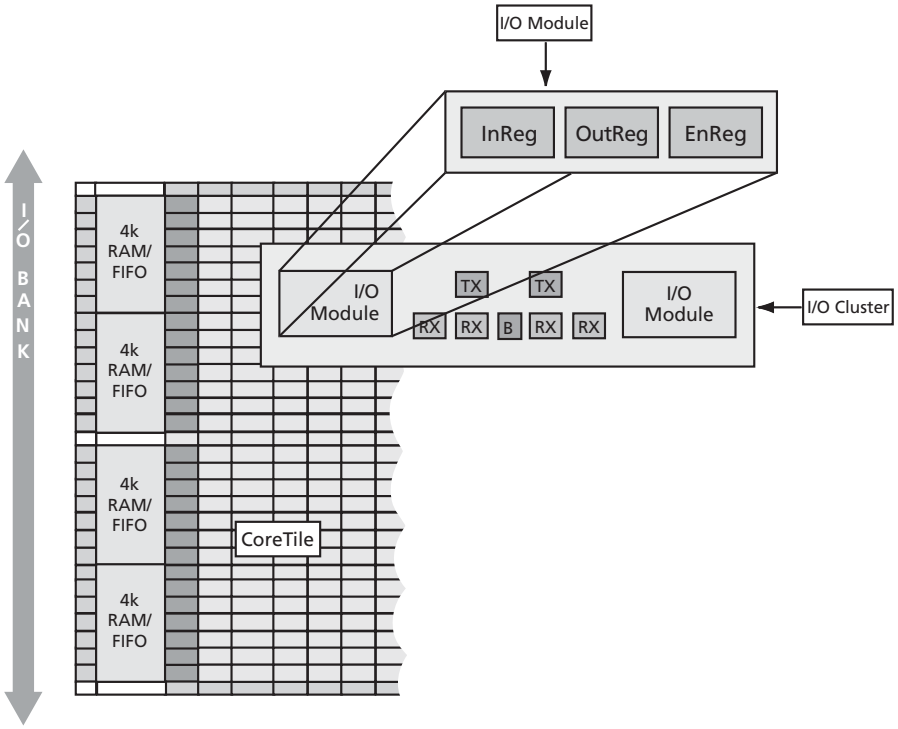


Figure 1-7 • **I/O Cluster Arrangement**

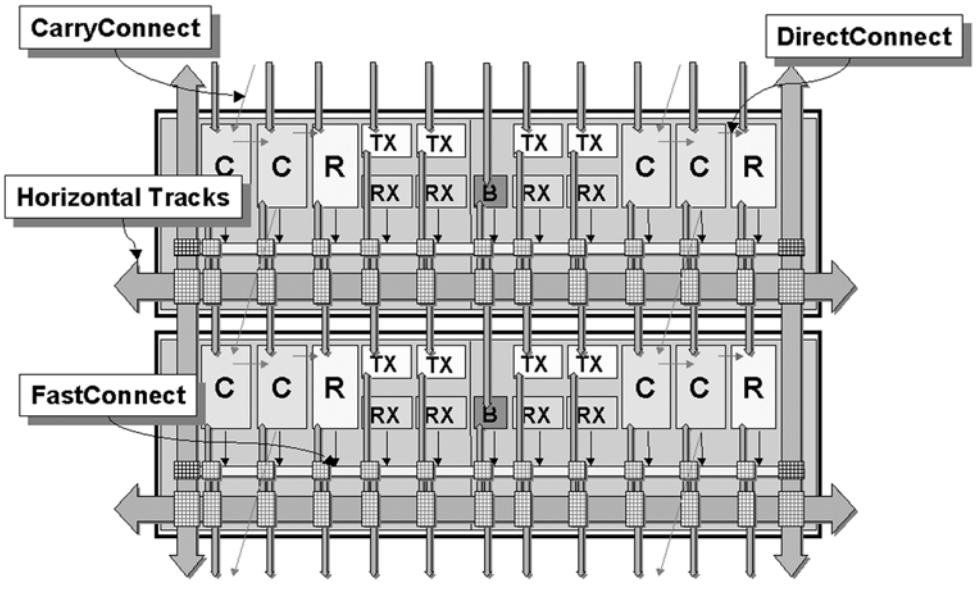


Figure 1-8 • **RTAX-S/SL Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-3). Both these clocks can be segmented, allowing significantly more than eight clock domains to be implemented in the devices.

The RTAX1000S/SL, RTAX2000S/SL, and RTAX4000S/SL devices have 12 HCLK segments per tile and 28 RCLK segments per tile. The RTAX250S/SL has 8 HCLK segments per tile and 22 RCLK segments per tile.

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Design Environment

The RTAX-S/SL family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the Libero IDE Flow diagram located on the Actel website). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, and Designer software from Actel.

Actel's Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor which support timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – allows the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, the Actel back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, the Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Programming support is provided through Actel Silicon Sculptor 3, a single-site programmer driven via a PC-based GUI. Factory programming is available for high-volume production needs.

Low-Cost Prototyping Solutions

Since the enhanced radiation characteristics of radiation-tolerant devices are not required during the prototyping phase of the design, Actel has developed two prototyping options for RTAX-S/SL. For early design development and functional verification, Actel offers the commercial Axcelerator devices while for final flight design verification in hardware, Actel offers the RTAX-S PROTO device that has the same form, fit, and function as the flight silicon.

Prototyping with Axcelerator Units

The prototyping solution using the commercial Axcelerator devices consists of two parts:

- A well-documented design flow that allows the customer to target an RTAX-S/SL design to the equivalent commercial Axcelerator device
- A set of Actel Extender circuit boards that map the commercial device package to the appropriate RTAX-S package footprint

This methodology provides the user with a cost-effective solution while maintaining the short time-to-market associated with Actel FPGAs.

Prototyping with RTAX-S PROTO Units

The RTAX-S PROTO units offer a prototyping solution that can be used for final timing verification of the flight design. The RTAX-S PROTO prototype units have the same timing attributes as the RTAX-S/SL flight units.

Prototype units are offered in non-hermetic ceramic packages. The prototype units include "PROTO" in their part number, and “PROTO” is marked on devices to indicate that they are not intended for space flight. They

also are not intended for applications, which require the quality of space-flight units, such as qualification of space-flight hardware. RT-PROTO units offer no guarantee of hermeticity, and no MIL-STD-883B processing. At a minimum, users should plan on using class B level devices for all qualification activities.

The RT-PROTO units are electrically tested in a manner to guarantee their performance over the full military temperature range. The RT-PROTO units will also be offered in -1 or standard speed grades, so as to enable customers to validate the timing attributes of their space designs using actual flight silicon.

Prototyping with ProASIC3E Reprogrammable Units

Using Actel's ProASIC3E prototyping solution offers the unique advantage of reprogrammability, resulting in cost savings while providing faster functional verification of designs in prototype stage. This methodology employs a footprint compatible adaptor board and an EDIF netlist and pinout convertor for easy migration.

Please see the application note *Prototyping for RTAX-S and RTAX-SL Devices* for more details.

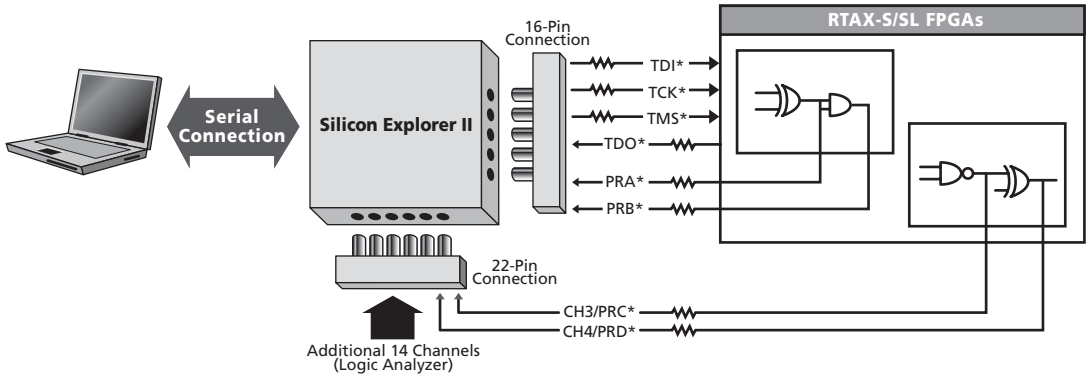
In-System Diagnostic and Debug Capabilities

The RTAX-S/SL family of FPGAs includes internal probe circuitry, allowing the designer to dynamically observe and analyze any signal inside the FPGA without disturbing normal device operation. Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled via Silicon Explorer II (Figure 1-9), the Actel integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA via the JTAG port (See "Silicon Explorer II Probe Interface" on page 2-102).

In addition, Actel offers a Configurable Logic Analyzer Module (CLAM), which allows a real-time verification and debug capability to be embedded into IP programmed into Actel FPGAs. CLAM allows signals from the inside of the IP core to be routed to the exterior of the chip for verification purposes.

Summary

The Actel RTAX-S/SL family of FPGAs extends the successful RTSX-SU family of radiation-tolerant FPGAs, adding embedded RAM, FIFOs, and high-speed I/Os. With the support of a suite of robust software tools, design engineers can incorporate high gate counts and fixed pins into an RTAX-S/SL design yet still achieve high performance and efficient device utilization in an SEU-hardened device.



Note: **Refer to the "Pin Descriptions" on page 2-11 for more information.*

Figure 1-9 • **Probe Setup**

Related Documents

Application Notes

Simultaneous Switching Noise and Signal Integrity
http://www.actel.com/documents/SSN_AN.pdf
Differences Between RTAX-S/SL and Axcelerator
http://www.actel.com/documents/RTAXS_AX_Features_AN.pdf
Using EDAC RAM for RadTolerant RTAX-S/SL FPGAs and Axcelerator FPGAs
http://www.actel.com/documents/EDAC_AN.pdf
Prototyping for RTAX-S and RTAX-SL Devices
http://www.actel.com/documents/PrototypingRTAXS_AN.pdf
Implementation of Security in Actel Antifuse FPGAs
http://www.actel.com/documents/Antifuse_Security_AN.pdf
Actel CQFP to FBGA Adapter Socket Instructions
http://www.actel.com/documents/CCGA_FBGA_AN.pdf
Actel CCGA to FBGA Adapter Socket Instructions
http://www.actel.com/documents/CQ352-FPGA_Adapter_AN.pdf
IEEE Standard 1149.1 (JTAG) in the Axcelerator Family
http://www.actel.com/documents/AX_JTAG_AN.pdf

User's Guides and Manuals

Antifuse Macro Library Guide
http://www.actel.com/documents/libguide_UG.pdf
SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder User's Guide
http://www.actel.com/documents/smarttime_ug.pdf
Silicon Sculptor User's Guide
http://www.actel.com/documents/SiliSculptII_Sculpt3_ug.pdf
Silicon Explorer II User's Guide
http://www.actel.com/documents/Silexpl_UG.pdf

White Papers

Design Security in Nonvolatile Flash and Antifuse FPGAs
http://www.actel.com/documents/DesignSecurity_WP.pdf
Understanding Actel Antifuse Device Security
http://www.actel.com/documents/AntifuseSecurityWP.pdf
RTAX-S/SL Testing and Reliability Update
http://www.actel.com/documents/RTAXS_Rel_Test_WP.pdf

Miscellaneous

Libero IDE flow diagram
http://www.actel.com/products/software/libero/#flow

Detailed Specifications

Table 2-1 • **I/O Features Comparison**

I/O Assignment	Clamp Diode	Hot Insertion / Cold Sparing	5V Tolerance	Input Buffer	Output Buffer
3.3 V LVTTL	Yes[1]	No	Yes[1]	Enabled/Disabled	
3.3 V PCI	Yes	No	Yes[2]	Enabled/Disabled	
LVCMOS2.5 V	No	Yes	No	Enabled/Disabled	
LVCMOS1.8 V	No	Yes	No	Enabled/Disabled	
LVCMOS1.5 V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled[3]
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled[4]

Notes:

1. *Default setting for the clamp diode is set to be PCI. The LVTTL clamp diode is not enabled by default. To allow 5 V tolerance, the LVTTL clamp diode needs to be enabled using settings in Designer. Hot-insertion and cold-sparing are not supported when the clamp diode is enabled.*
2. *Can be implemented with an external resistor.*
3. *The OE input of the output buffer is automatically deasserted by Designer.*
4. *The OE input of the output buffer is automatically asserted by Designer.*

5 V Tolerance

3.3 V PCI and 3.3 V LVTTL (with clamp diode enabled) I/O standards directly allow 5 V tolerance. For example, the 3.3V PCI I/O standard provides an internal clamp diode between the input pad and the V_{CCI} pad so that the voltage at the input pin is clamped below the absolute maximum input voltage of 4.1 V (Table 2-2 on page 2-2). An example of the input pad voltage level is shown in EQ 2-1:

$$V_{input} = V_{CCI} + V_{diode} = 3.3\ V + 0.7\ V = 4.0\ V$$

EQ 2-1

The internal clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the V_{CCI} is powered off. An external series resistor (~100 Ω) is required between the input pin and the 5 V signal source to limit the current to less than 20 mA (Figure 2-1). The 100 Ω resistor was chosen to meet the input Tr/Tf requirement (Table 2-20 on page 2-22).

5 V tolerance is not allowable for V_{CCI} greater than 3.3 V or for input signals greater than 5.0 V.

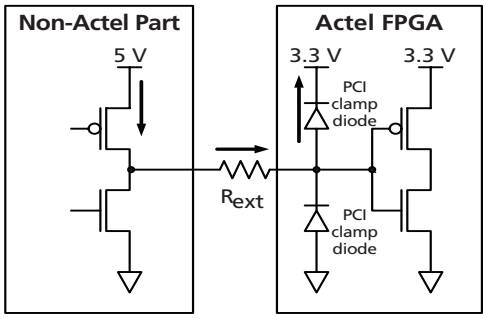


Figure 2-1 • **Use of an External Resistor for 5 V Tolerance**

Operating Conditions

Absolute Maximum Conditions

Stresses beyond those listed in Table 2-2 may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions in Table 2-3.

Table 2-2 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
T_J	Junction Temperature	–55 to +135	°C
V_{CCA}	AC Core Supply Voltage[1]	–0.3 to 1.8	V
V_{CCA}	DC Core Supply Voltage	–0.3 to 1.7	V
V_{CCI}	DC I/O Supply Voltage	–0.3 to 3.75	V
V_{REF}	DC I/O Reference Voltage	–0.3 to 3.75	V
V_I	Input Voltage	–0.5 to 4.1	V
V_O	Output Voltage	–0.5 to 3.75	V
T_{STG}	Storage Temperature	–60 to +150	°C
V_{CCDA}[2]	Supply Voltage for Differential I/Os	–0.3 to 3.75	V
V_{PUMP}	Supply Voltage for External Pump	–0.3 to 3.75	V

Notes:

1. *The AC transient V_{CCA} limit is for radiation-induced transients less than 10 µs duration and not intended for repetitive use. Core voltage spikes from a single event transient will not negatively affect the reliability of the device if, for this non-repetitive event, the transient does not exceed 1.8 V at any time and the total time that the transient exceeds 1.575 V does not exceed 10 µs in duration.*
2. *V_{CCDA} must be greater than or equal to the highest V_{CCI} voltage*

Table 2-3 • **RTAX-S/SL Recommended Operating Conditions**

Parameter Range	Military	Units
Junction Temperature (T_J)	–55 to +125	°C
Ambient Temperature (T_A)[1]	–55 to +125	°C
1.5 V Core Supply Voltage	1.425 to 1.575	V
1.5 V I/O Supply Voltage	1.425 to 1.575	V
1.8 V I/O Supply Voltage	1.71 to 1.89	V
2.5 V I/O Supply Voltage	2.375 to 2.625	V
3.3 V I/O Supply Voltage	3.0 to 3.6	V
2.5 V V_{CCDA} I/O Supply Voltage (no differential I/O used)	2.375 to 2.625	V
3.3 V V_{CCDA} I/O Supply Voltage (differential or voltage-referenced I/O used)[2]	3.0 to 3.6	V
3.3 V V_{PUMP} Supply Voltage	3.0 to 3.6	V

Notes:

1. *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.*
2. *Please see "VCCDA Supply Voltage" on page 2-11 more detail.*

Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to –1.0 V for no longer than 10% of the period or 11 ns (whichever is smaller). Current during the transition must not exceed 95 mA.

For AC signals, the input signal may overshoot during transitions to V_{CCI} + 1.0 V for no longer than 10% of the period or 11 ns (whichever is smaller). Current during the transition must not exceed 95 mA.

Note: The above specification does not apply to the PCI standard. The RTAX-S/SL PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

Power-Up/Down Sequence

V_{CCA}, V_{CCI}, and V_{CCDA} can be powered up or powered down in any sequence. During power-up, all RTAX-S/SL I/Os are tristated until they reach the state defined by the design.

Calculating Power Dissipation

Table 2-4 • **RTAX-S Standby Current**

Device	Temperature	I_{CCA} (mA)	I_{CCI} (mA)	I_{CCDA} (mA)	$I_{CCDIFFA}$ (mA)	I_{IH}, I_{IL}, I_{OZ} (µA)[1]
RTAX4000S	Typical 25°C	75	15	15	3.13	1
	125°C	600	60	20	3.7	5
RTAX2000S	Typical 25°C	50	10	7	3.13	1
	125°C	500	35	10	3.7	5
RTAX1000S	Typical 25°C	30	10	7	3.13	1
	125°C	450	35	10	3.7	5
RTAX250S	Typical 25°C	20	5	5	3.13	1
	125°C	250	20	10	3.7	5

Notes:

1. *I_{IH}, I_{IL}, or I_{OZ} values are measured with inputs at the same level as V_{CCI} for I_{IH} and GND for I_{IL} and I_{OZ}.*
2. *Above values are maximum.*
3. *Values in the $I_{CCDIFFA}$ column refer to the current (in addition to I_{CCDA}) flowing per pair through differential amplifiers only when using differential pairs or voltage references pins.*

Table 2-5 • **RTAX-SL Standby Current**

Device	Temperature	I_{CCA} (mA)	I_{CCI} (mA)	I_{CCDA} (mA)	$I_{CCDIFFA}$ (mA)	I_{IH}, I_{IL}, I_{OZ} (µA)[1]
RTAX4000SL	Typical 25°C	40	15	15	3.13	1
	125°C	300	60	20	3.7	5
RTAX2000SL	Typical 25°C	30	10	7	3.13	1
	125°C	150	35	10	3.7	5
RTAX1000SL	Typical 25°C	20	10	7	3.13	1
	125°C	90	35	10	3.7	5
RTAX250SL	Typical 25°C	15	5	5	3.13	1
	125°C	60	20	10	3.7	5

Notes:

1. *I_{IH}, I_{IL}, or I_{OZ} values are measured with inputs at the same level as V_{CCI} for I_{IH} and GND for I_{IL} and I_{OZ}.*
2. *Above values are maximum.*
3. *Values in the $I_{CCDIFFA}$ column refer to the current (in addition to I_{CCDA}) flowing per pair through differential amplifiers only when using differential pairs or voltage references pins.*

Table 2-6 • **Default C_{load} / V_{CCI}**

	C_{load} (pF)	V_{CCI} (V)	P_{load} (µW/MHz)	P_{10} (µW/MHz)	$P_{I/O}$ (µW/MHZ)*
Single-Ended without V_{REF}					
LVCMOS – 15 (JESD8-11)	35	1.5	78.8	49.5	128.3
LVCMOS –18	35	1.8	113.4	73.4	186.8
LVCMOS – 25	35	2.5	218.8	148.0	366.8
LVTTL 8 mA Low Slew	35	3.3	381.2	118.7	499.9
LVTTL 12 mA Low Slew	35	3.3	381.2	138.6	519.8
LVTTL 16 mA Low Slew	35	3.3	381.2	150.8	532.0
LVTTL 24 mA Low Slew	35	3.3	381.2	169.2	550.4
LVTTL 8 mA High Slew	35	3.3	381.2	130.3	511.5
LVTTL 12 mA High Slew	35	3.3	381.2	165.9	547.1
LVTTL 16 mA High Slew	35	3.3	381.2	225.1	606.3
LVTTL 24 mA High Slew	35	3.3	381.2	267.5	648.7
PCI	10	3.3	108.9	218.5	327.4
PCI-X	10	3.3	108.9	162.9	271.8
Single-Ended with V_{REF}					
SSTL2-I	30	2.5	–	171.2	171.2
SSTL2-II	30	2.5	–	147.8	147.8
SSTL3-I	30	3.3	–	327.2	327.2
SSTL3-II	30	3.3	–	288.4	288.4
HSTL-I	20	1.5	–	40.9	40.9
GTLP – 33	10	3.3	–	68.5	68.5
Differential					
LVPECL – 33	N/A	3.3	–	260.6	260.6
LVDS – 25	N/A	2.5	–	145.8	145.8

Note: $*P_{I/O} = P_{10} + C_{load} * V_{CCI}^2$

Table 2-7 • **Different Components Contributing to the Total Power Consumption in RTAX-S/SL Devices**

Symbol	Power Component	Device-Specific Value (in µW/MHz)			
		RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
P1	Core tile HCLK power component	85.8	227.5	378.0	700
P2	R-cell power component	0.6	0.6	0.6	0.6
P3	HCLK signal power dissipation	7.7	23.2	31.0	50
P4	Core tile RCLK power component	1.8	227.5	378.0	700
P5	R-cell power component	0.9	0.9	0.9	0.9
P6	RCLK signal power dissipation	8.6	25.7	34.3	55
P7	Power dissipation due to the switching activity on the R-cell	1.6	1.6	1.6	1.6
P8	Power dissipation due to the switching activity on the C-cell	1.4	1.4	1.4	1.4
P9	Power component associated with input voltage	10.0	10.0	10.0	10
P10	Power component associated with output voltage	See Table 2-4 and Table 2-5 on page 2-3 for per pin contribution.			
P11	Power component associated with the read operation in the RAM block	25.0	25.0	25.0	25.0
P12	Power component associated with the write operation in the RAM block	30.0	30.0	30.0	30.0

$P_{total} = P_{dc} + P_{ac}$

$P_{dc} = I_{CCA} * V_{CCA} + I_{CCI} * V_{CCI} + I_{CCDA} * V_{CCDA} + I_{CCDIFFA} * V_{CCDA} * N_{b\_da\_pairs}$

$P_{ac} = P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory}$

$N_{b\_da\_pairs}$ = number of differential pairs or voltage referenced pins used

$P_{HCLK} = (P1 + P2 * s + P3 * sqrt[s]) * Fs$

s = number of R-cells clocked by this clock

Fs = clock frequency

$P_{CLK} = (P4 + P5 * s + P6 * sqrt[s]) * Fs$

s = number of R-cells clocked by this clock

Fs = clock frequency

$P_{R\text{-}cells} = P7 * ms * Fs$

ms = number of R-cells switching at each Fs cycle

Fs = clock frequency

$P_{C\text{-}cells} = P8 * mc * Fs$

mc = number of C-cells switching at each Fs cycle

Fs = clock frequency

$P_{inputs} = P9 * pi * F_{pi}$

pi = number of inputs

F_{pi} = average input frequency

$P_{outputs} = (P10 + C_{load} * V_{CCI}^2) * po * F_{po}$

C_{load} = output load (technology dependent)

V_{CCI} = output voltage (technology dependent)

po = number of outputs

F_{po} = average output frequency

$P_{memory} = P11 * N_{block} * F_{RCLK} + P12 * N_{block} * F_{WCLK}$

N_{block} = number of RAM/FIFO blocks (1 block = 4k)

F_{RCLK} = read-clock frequency of the memory

F_{WCLK} = write-clock frequency of the memory

Power Estimation Example

This example employs an RTAX1000S/SL shift-register design with 1,080 R-cells, one C-cell, one reset input, and one output. This design also uses a single clock (HCLK) at 100 MHz and is operated under room temperature.

ms = 1,080 (in a shift register 100% of R-cells are toggling at each clock cycle)

Fs = 100 MHz

s = 1,080

=> $P_{HCLK} = (P1 + P2 * s + P3 * sqrt[s]) * Fs = 163.8$ mW

and Fs = 100 MHz

=> $P_{R\text{-}cells} = P7 * ms * Fs = 172.8$ mW

mc = 1 (1 C-cell in this design)

and Fs = 100 MHz

=> $P_{C\text{-}cells} = P8 * mc * Fs = 0.14$ mW

F_{pi} ~ 0 MHz

and pi= 1 (1 reset input => this is why $F_{pi} = 0$)

=> $P_{inputs} = P9 * pi * F_{pi} = 0$ mW

F_{po} = 50 MHz

C_{load} = 35 pF

V_{CCI}= 3.3 V

and po = 1

=> $P_{outputs} = (P10 + C_{load} * V_{CCI}^2) * po * F_{po} = 23.6$ mW

No RAM/FIFO in this shift-register

=> $P_{memory} = 0$ mW

$P_{ac} = P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} = 360.4$ mW

$P_{dc} = I_{CCA} * V_{CCA} + I_{CCI} * V_{CCI} + I_{CCDA} * V_{CCDA} + I_{CCDIFFA} * V_{CCDA} * N_{b\_da\_pairs} = 101.1$ mW

$P_{total} = P_{dc} + P_{ac} = 360.4$ mW + 101.1 mW = 461.5 mW

Thermal Characteristics

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient, case or board temperature. This is an important distinction because dynamic and static power consumption causes the chip's junction temperature to be higher than the ambient, case or board temperature. EQ 2-2, EQ 2-3, and EQ 2-4 show the relationship between thermal resistance, temperature, and power.

$$\theta_{ja} = \frac{T_j - T_a}{P} \quad \text{EQ 2-2}$$

$$\theta_{jc} = \frac{T_j - T_c}{P} \quad \text{EQ 2-3}$$

$$\theta_{jb} = \frac{T_j - T_b}{P} \quad \text{EQ 2-4}$$

Where:

θ_{ja} = Thermal resistance from junction to air
θ_{jc} = Thermal resistance from junction to case
θ_{jb} = Thermal resistance from junction to board
T_j = Junction Temperature
T_a = Ambient Temperature
T_c = Case Temperature
T_b = Board Temperature
P = Power

Table 2-8 • **Package Thermal Characteristics**

Product	Package Type	θ_{ja}	θ_{jc}	θ_{jb}	Units
RTAX250S/SL	CQ208	19.9	0.8	N/A	C/W
	CQ352	16.8	0.7	N/A	C/W
	CG624	13.7	TBD	TBD	C/W
RTAX1000S/SL	CQ352	13.3	0.4	N/A	C/W
	CG624	10.8	5.6	4.5	C/W
RTAX2000S/SL	CQ256	15.8	0.25	N/A	C/W
	CQ352	12.3	0.2	N/A	C/W
	CG624	9.7	4.3	3.5	C/W
	CG1152	9.0	2.0	2.6	C/W
RTAX4000S/SL	CQ352	12.3	0.2	N/A	C/W
	CG1272	8.0	2.0	2.2	C/W

Notes:

1. *θ_{ja} are estimated at still air.*
2. *θ_{jc} for CQFP refers to the thermal resistance between the junction and the bottom surface of the package.*
3. *θ_{jc} for CG packages refers to the thermal resistance between the junction and the top surface of the package.*
4. *The θ_{jb} values in the table are simulated under conduction heat transfer only.*

Calculation for Power

Sample Case 1: Convection ≠ 0

A sample calculation of the power dissipation allowed for an RTAX1000S/SL-CG624 in still air is shown below. Assume that the maximum junction temperature is maintained at 110°C and the ambient temperature is 50°C. The maximum power allowed can be estimated using the equation below.

T_j = 110°C

T_a = 50°C

$$\theta_{ja} = 10.8°C/W = \frac{110°C - 50°C}{P}$$

P = 5.55 W

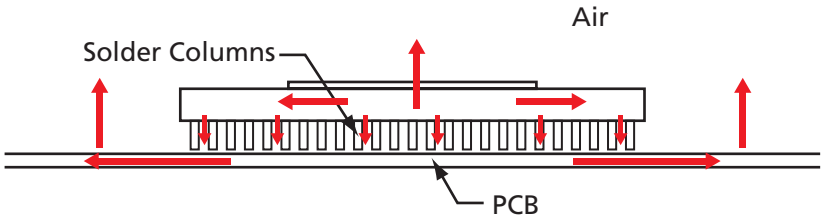


Figure 2-2 • **Heat Flow when Air is Present**

Sample Case 2: Convection = 0

A sample calculation of the power dissipation when there is no air in the environment is shown below. An RTAX1000S/SL-CQ352 is attached to the board with a thermal adhesive between the package body. The thermal resistance of the paste is 0.58°C/W. Since air is not present in the environment, most of the heat will be flowing through the bottom of the package, through the thermal paste, and to the board. Neglecting the heat flowing through the package leads, the maximum power allowed can be estimated as shown in the equations below.

T_j = 110°C

θ_{cb} = Thermal resistance of the thermal paste from case to board (i.e., = 0.58°C/W)

T_b = 70°C

$$\theta_{jb\ (Total)} = \theta_{jc} + \theta_{cb}$$

$$\theta_{jc} + \theta_{cb} = \frac{110°C - 70°C}{P}$$

$$0.4°C/W + 0.58°C/W = \frac{110°C - 70°C}{P}$$

$$\theta_{jb\ (Total)} = \frac{110°C - 70°C}{P}$$

P = 40.8 W

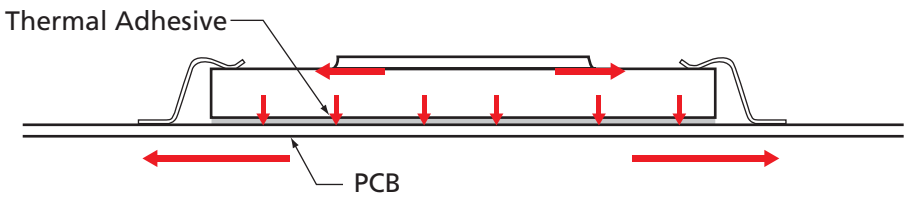


Figure 2-3 • **Heat Flow in a Vacuum**

The thermal resistances, shown in Table 2-8 on page 2-7, are based on the simulations done with test conditions and test boards configurations specified in JEDEC specification JESD51.

Timing Characteristics

RTAX-S/SL devices are manufactured in a CMOS process, therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in Table 2-9 should be applied to all timing data contained within this datasheet.

Table 2-9 • **Temperature and Voltage Timing Derating Factors (Normalized to Worst-Case Military, T_J = 125°C, V_{CCA} = 1.4 V)**

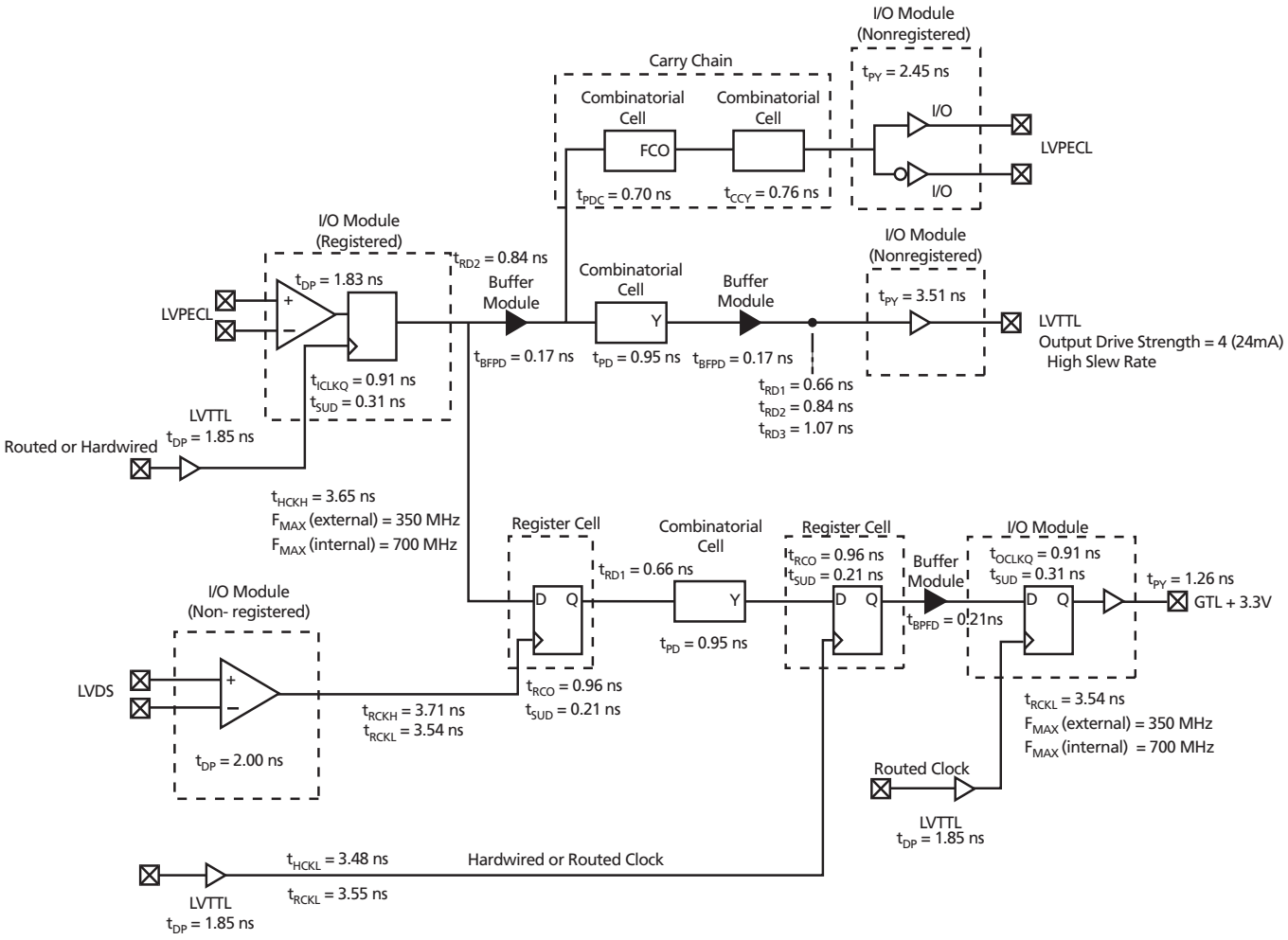
	Junction Temperature						
V_{CCA}	**–55°C**	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
1.4V	0.74	0.75	0.80	0.84	0.89	0.92	1.00
1.425V	0.72	0.74	0.79	0.82	0.88	0.91	0.98
1.5V	0.69	0.71	0.75	0.78	0.84	0.86	0.94
1.575V	0.66	0.68	0.72	0.75	0.80	0.83	0.90
1.6V	0.65	0.67	0.71	0.74	0.79	0.82	0.89

Notes:

1. *The user can set the junction temperature in Designer software to be any integer value in the range of –55°C to 125°C.*
2. *The user can set the core voltage in Designer software to be any value between 1.4V and 1.6V.*

All timing numbers listed in this datasheet represent sample timing characteristics of RTAX-S/SL devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Actel's Designer software after place-and-route.

Timing Model



Note: *Timing data is for the RTAX2000S/SL, –1 speed.*

Figure 2-4 • **Timing Model**

Hardwired Clock[1]

External Setup

= $(t_{DP} + t_{RD2} + t_{SUD}) - t_{HCKH}$

= (1.85 + 0.84 + 0.31) – 3.65

= –0.61

Clock-to-Out (Pad-to-Pad)

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{PY}$

= 3.65 + 0.96 + 0.66 + 3.51

= 8.78 ns

Routed Clock[1]

External Setup

= $(t_{DP} + t_{RD2} + t_{SUD}) - t_{RCKH}$

= (1.85 + 0.84 + 0.31) – 3.54

= –0.71 ns

Clock-to-Out (Pad-to-Pad)

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{PY}$

= 3.71 + 0.96 + 0.66 + 3.51

= 8.84 ns

1. *Calculations are examples of how to calculate related parameters and do not necessary match the path represented in the "Timing Model".*

I/O Specifications

Pin Descriptions

Supply Pins

GND **Ground**

Low supply voltage.

V_{CCA} **Supply Voltage**

Supply voltage for array (1.5 V).

V_{CCIBx} **Supply Voltage**

Supply voltage for I/Os. Bx is the I/O Bank ID – 0 to 7. See "User I/Os" on page 2-12 for more information. Unused V_{CCI}BX I/O banks may be tied to GND or can be tied to other used V_{CCI}BX I/O banks within the same device.

V_{CCDA} **Supply Voltage**

Supply voltage for the I/O differential amplifier and JTAG and probe interfaces. V_{CCDA} is either 3.3 V or 2.5 V and must use 3.3 V when voltage-referenced and/or differential is used. Additionally, V_{CCDA} must be greater than or equal to any V_{CCI} voltages (i.e. $V_{CCDA} \geq V_{CCI}$Bx).

V_{PUMP} **Supply Voltage (External Pump)**

In low-power mode, V_{PUMP} will be used to access an external charge pump (if the user desires to bypass the internal charge pump to further reduce power). The device starts using the external charge pump when the voltage level on V_{PUMP} reaches 3.3 V.[2] In normal device operation, when using the internal charge pump, V_{PUMP} can be directly tied or through a 1K resistor to GND.

User-Defined Supply Pins

V_{REF} **Supply Voltage**

Reference voltage for I/O banks. V_{REF} pins are configured by the user from regular I/O pins; V_{REF} are not in fixed locations. There can be one or more V_{REF} pins in an I/O bank.

Global Pins

HCLKA/B/C/D **Dedicated (Hardwired) Clocks A, B, C, and D**

These pins are the clock input for sequential modules. Input levels are compatible with all supported I/O standards (there is a P/N pin pair for support of differential I/O standards). This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. HCLK pins may be used either as HCLK inputs or as user I/Os. If they are not being used for either purpose, Actel recommends that they are tied to ground.

CLKE/F/G/H **Global Clocks E, F, G, and H**

These pins are clock inputs for clock distribution networks. Input levels are compatible with all supported I/O standards (there is a P/N pin pair for support of differential I/O standards). The clock input is buffered prior to clocking the R-cells. CLK pins may be used either as CLK inputs or as user I/Os. If they are not being used for either purpose, Actel recommends that they are tied to a known state.

2. When V_{PUMP} = 3.3V, it shuts off the internal charge pump.

JTAG/Probe Pins

PRA/B/C/D[3] **Probes A, B, C, and D**

The dedicated probe pins are used to output data from any user-defined design node within the device (controlled with Silicon Explorer II). These independent diagnostic pins can be used to allow real-time diagnostic output of any signal path within the device. The pins' probe capabilities can be permanently disabled to protect programmed design confidentiality. Refer to Table 2-102 on page 2-100 for recommendations on pin status for flight boards.

TCK[2] **Test Clock**

Test clock input for JTAG boundary-scan testing and diagnostic probe (Silicon Explorer II).

TDI[2] **Test Data Input**

Serial input for JTAG boundary-scan testing and diagnostic probe. TDI is equipped with an internal pull-up resistor with approximately 10 kΩ resistance.

TDO[2] **Test Data Output**

Serial output for JTAG boundary-scan testing.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 boundary-scan pins (TCK, TDI, TDO, TRST). TMS is equipped with an internal pull-up resistor with approximately 10 kΩ resistance.

TRST **Boundary Scan Reset Pin**

The TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with a programmable pull-up resistor with approximately 10 kΩ resistance (i.e. with or without the pull-up resistor). This pin must be hardwired to ground for flight.

Special Functions

NC **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

User I/Os[4]

Introduction

The RTAX-S/SL family features a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) with its bank-selectable I/Os. Table 2-10 on page 2-13 contains the I/O standards supported by the RTAX-S/SL family.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristated value of Hi-Z)
- Input buffer is disabled (with tristated value of Hi-Z)
- No pull-up/pull-down is programmed

In Actel Designer Software, unused RTAX-S/SL I/Os are configured as tristate with no pull-up resistors.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits.

All I/O standards are 3.3 V tolerant, and I/O standards, except 3.3 V PCI, are capable of hot insertion and cold sparing. 3.3 V PCI is also 5 V tolerant with the aid of an external resistor (see "5 V Tolerance" on page 2-1).

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). By design, all user flip-flops in the RTAX-S/SL FPGAs are immune to SEUs including the following three registers located in every I/O cell buffer: InReg, OutReg, and EnReg.

I/Os are organized into banks, and there are eight banks per device – two per side (Figure 2-7 on page 2-21). Each I/O bank has a common V_{CCI}, the supply voltage for its I/Os.

3. *Actel recommends that you use a series termination resistor on every probe connector (TDI, TCK, TDO, PRA, PRB, PRC, and PRD). The series termination is used to prevent data transmission corruption (i.e., due to reflection from the FPGA to the probe connector) during probing and reading back the checksum. With an internal setup we have seen 70-ohm termination resistor improved the signal transmission. Since the series termination depends on the setup, Actel recommends users to calculate the termination resistor for their own setup. Below is a guideline on how to calculate the resistor value.*
   The resistor value should be chosen so that the sum of it and the probe signal's driver impedance equals the effective trace impedance.
   Z0 = Rs + Zd
   Z0 = trace impedance (silicon explorer's breakout cable's resistance + PCB trace impedance), Rs = series termination,
   Zd = probe signal's driver impedance.
   The termination resistor should be placed as close as possible to the driver.
   Among the probe signals, TDI, TCK, and TMS are driven by Silicon Explorer. A54SX16 is used in Silicon Explorer and hence the driver impedances needs to be calculated from RTAX-S IBIS Models (Mixed Voltage Operation). PRA, PRB, PRC, PRD, and TDO are driven by the FPGA and driver impedance can also be calculated from the IBIS Model.
   Silicon explorer's breakout cable's resistance is usually close to 1 ohm.
4. *Do not use an external resistor to pull the I/O above V_{CCI} for a higher logic "1" voltage level. The desired higher logic "1" voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above V_{CCI}.*

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, V_{REF}. While V_{REF} must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a V_{REF}.

The location of the V_{REF} pin should be selected according to the following rules:

- Any pin that is assigned as a V_{REF} can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank.
- I/O package locations listed as no-connects are counted as part of the 16 maximum. In many cases, this leads to fewer than eight user I/O package pins in each direction being controlled by a V_{REF} pin.
- Dedicated I/O pins (GND, V_{CCI}...) are not counted as part of the 16.
- The user I/O pad immediately adjacent on either side of the V_{REF} pin may only be used as an input. The exception is when there is a V_{CCI}/GND pair separating the V_{REF} pin and the user I/O pad location.

The differential amplifier supply voltage V_{CCDA} should be connected to 3.3 V. When neither voltage-referenced nor differential I/Os are used, V_{CCDA} may be connected to 2.5 V when V_{CCI} <= 2.5 V in a given I/O bank; however, it is still recommended to connect V_{CCDA} to 3.3 V.

The user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard
- Use generic I/O macros and then use Actel Designer's PinEditor to specify the desired I/O standards. (Please note that this is not applicable to differential standards.)
- A combination of the first two methods

Please refer to the *I/O Features in Axcelerator Family Devices* application note and the *Antifuse Macro Library Guide* for more details.

Table 2-10 • **I/O Standards Supported by the RTAX-S/SL Family**

I/O Standard	Input/Output Supply Voltage (V_{CCI})	Input Reference Voltage (V_{REF})	Board Termination Voltage (V_{TT})
LVTTL	3.3	N/A	N/A
LVCMOS 2.5 V	2.5	N/A	N/A
LVCMOS 1.8 V	1.8	N/A	N/A
LVCMOS 1.5 V (JDEC8-11)	1.5	N/A	N/A
3.3 V PCI	3.3	N/A	N/A
GTL+ 3.3 V	3.3	1.0	1.2
GTL+ 2.5 V*	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

Note: ** 2.5 V GTL+ is not supported across the full military temperature range.*

Simultaneous Switching Outputs (SSO)

Actel defines SSOs as any outputs that transition in phase within a 1 ns window. The measurements made by Actel are based on the following worst-case conditions:

1. The switching outputs are adjacent to the quiet output on either side.
2. All unused I/O buffers are tristated so they do not help either ground or V_{CC}.
3. A worst-case package was used.

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the RTAX-S/SL family.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (V_{REF}) and an input/output supply voltage (V_{CCI}), only I/Os with compatible standards can be assigned to the same bank.

Table 2-11 shows the compatible I/O standards for a common V_{REF} (for voltage-referenced standards). Similarly, Table 2-12 shows compatible standards for a common V_{CCI}.

Table 2-11 • **Compatible I/O Standards for Different V_{REF} Values**

V_{REF}	Compatible Standards
1.5 V	SSTL 3 (Class I and II)
1.25 V	SSTL 2 (Class I and II)
1.0 V	GTL+ (2.5 V and 3.3 V Outputs)
0.75 V	HSTL (Class I)

Table 2-12 • **Compatible I/O Standards for Different V_{CCI} Values**

V_{CCI} [1]	Compatible Standards	V_{REF}
3.3 V	LVTTL, PCI, LVPECL, GTL+ 3.3V	1.0
3.3 V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5 V	LVCMOS 2.5V, GTL+ 2.5V, LVDS[2]	1.0
2.5 V	LVCMOS 2.5V, SSTL 2 (Classes I and II), LVDS[2]	1.25
1.8 V	LVCMOS 1.8V	N/A
1.5 V	LVCMOS 1.5V, HSTL Class I	0.75

Notes:

1. *V_{CCI} is used for both inputs and outputs.*
2. *V_{CCI} tolerance is* ±5%.

Table 2-13 on page 2-15 summarizes the different combinations of voltages and I/O standards that can be used together in the same I/O bank. Note that two I/O standards are compatible if:

- Their V_{CCI} values are identical
- Their V_{REF} standards are identical (if applicable)

For example, if LVTTL 3.3 V (V_{REF}= 1.0V) is used, then the other available (i.e. compatible) I/O standards in the same bank are LVTTL 3.3 V PCI, GTL+, and LVPECL.

Also note that when multiple I/O standards are used within a bank, the voltage tolerance will be limited to the minimum tolerance of all I/O standards used in the bank. For instance, when using LVCMOS2.5 (+/-8% V_{CCI} tolerance) and LVDS (+/-5% V_{CCI} tolerance) within an I/O bank, the maximum voltage tolerance of the bank will be +/-5% V_{CCI}.

Table 2-13 • **Legal I/O Usage Matrix**

I/O Standard	LVTTL 3.3 V	LVCMOS 2.5 V	LVCMOS1.8 V	LVCMOS1.5 V (JESD8-11)	3.3 V PCI	GTL + (3.3 V)	GTL + (2.5 V)	HSTL Class I (1.5 V)	SSTL2 Class I & II (2.5 V)	SSTL3 Class I & II (3.3 V)	LVDS (2.5 V ±5%)	LVPECL (3.3 V)
LVTTL 3. 3V (V_{REF}=1.0V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVTTL 3. 3V(V_{REF}=1.5V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVCMOS 2.5 V (V_{REF}=1.0V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVCMOS 2.5 V (V_{REF}=1.25V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVCMOS1.8 V	–	–	✓	–	–	–	–	–	–	–	–	–
LVCMOS1.5 V (V_{REF}=1.75 V) (JESD8-11)	–	–	–	✓	–	–	–	✓	–	–	–	–
3.3 V PCI (V_{REF}=1.0V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
3.3 V PCI (V_{REF}=1.5V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
GTL+ (3.3 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
GTL+ (2.5 V)	–	✓	–	–	–	–	✓	–	–	–	–	–
HSTL Class I	–	–	–	✓	–	–	–	✓	–	–	–	–
SSTL2 Class I & II	–	✓	–	–	–	–	–	–	✓	–	✓	–
SSTL3 Class I & II	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVDS (V_{REF}=1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVDS (V_{REF}=1.25 V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVPECL (V_{REF}=1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVPECL (V_{REF}=1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓

Notes:

1. *Note that GTL+2.5 V is not supported across the full military temperature range.*
2. *A "✓" indicates whether standards can be used within a bank at the same time.*
   Examples:
   a) LVTTL can be used with 3.3 V PCI and GTL+ (3.3 V), when V_{REF} = 1.0 V (GTL+ requirement).
   b) LVTTL can be used with 3.3 V PCI and SSTL3 Class I and II, when V_{REF} = 1.5 V (SSTL3 requirement).
   c) LVDS V_{CCI} = 2.5 V ±5%.

I/O Clusters

Each I/O cluster incorporates two I/O modules, four RX modules and two TX modules, and a buffer module. In turn, each I/O module contains one Input Register (InReg), one Output Register (OutReg), and one Enable Register (EnReg) (Figure 2-5).

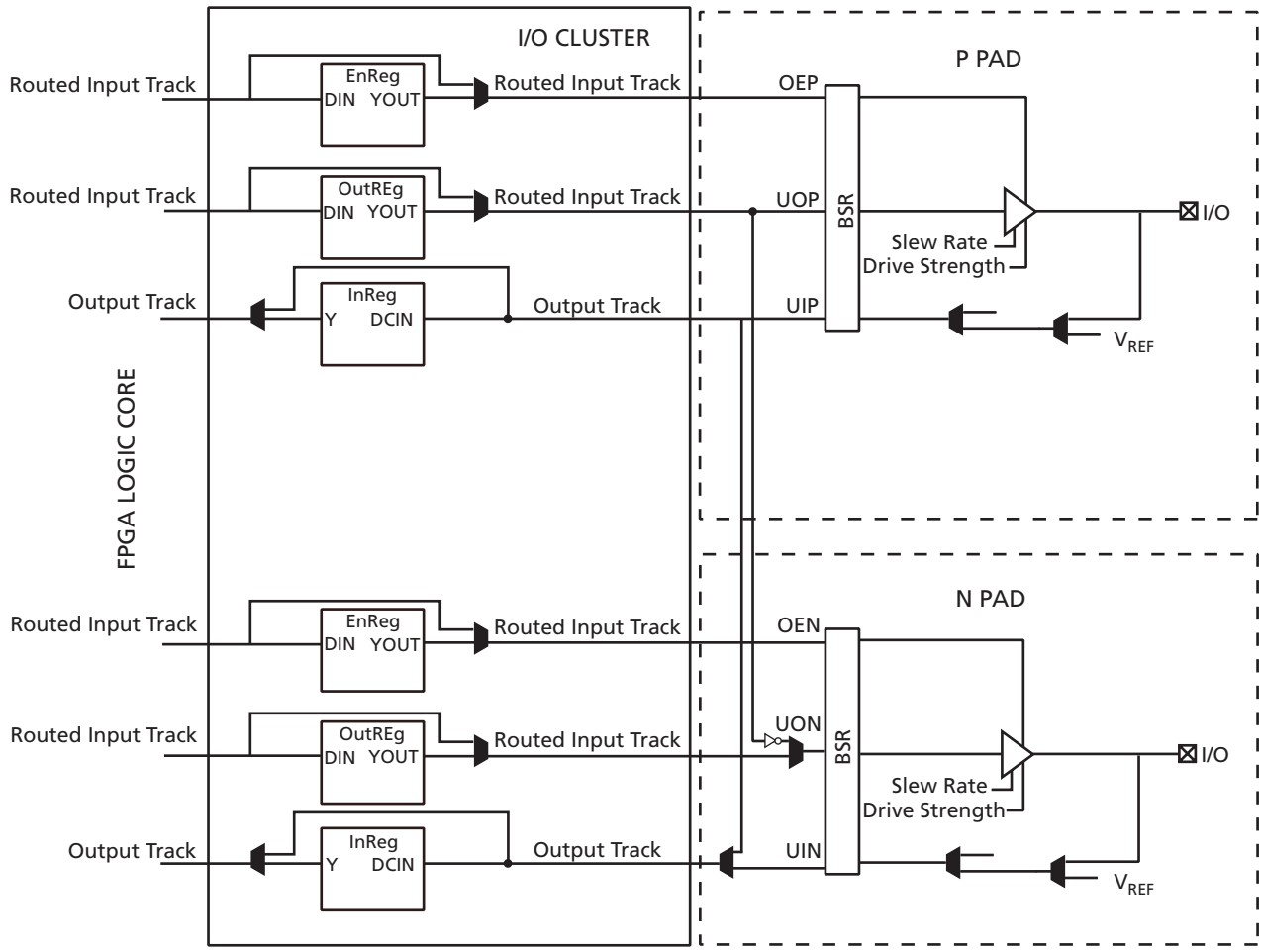


Figure 2-5 • **I/O Cluster Interface**

Using an I/O Register

To access the I/O registers, registers must be instantiated in the netlist and then connected to the I/Os. Usage of each I/O register (register combining) is individually controlled and can be selected/deselected using the PinEditor tool in Actel's Designer software. I/O register combining can also be controlled at the device level, affecting all I/Os. Please note, the I/O register option is deselected by default in any given design.[5]

In addition, Designer software provides a global option to enable/disable the usage of registers in the I/Os. This option is design specific. The setting for each individual I/O overrides this global option. Furthermore, the Global Set Fuse option in the Designer software, when checked, causes all I/O registers to output logic HIGH at device power-up.

Using the Weak Pull-Up and Pull-Down Circuits

Each RTAX-S/SL I/O comes with a weak pull-up/down circuit (on the order of 10 kΩ). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5 V, 1.8 V, and 1.5 V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

5. *Please note that register combining for multi fanout nets is not supported.*

Customizing the I/O

- A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis (Table 2-14). It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.
- The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.
- The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values – 8mA, 12mA, 16mA, or 24mA – that can be specified in Designer.[6]

Table 2-14 • **Bank Wide Delay Values**

	–1	Std.
Bit Setting	**Delay (ns)**	
0	0.88	1.03
1	1.10	1.29
2	1.21	1.42
3	1.44	1.69
4	1.53	1.80
5	1.75	2.06
6	1.86	2.19
7	2.09	2.46
8	2.16	2.54
9	2.38	2.80
10	2.49	2.93
11	2.72	3.20
12	2.81	3.30
13	3.04	3.57
14	3.15	3.70
15	3.37	3.96
16	3.39	3.98
17	3.61	4.25
18	3.72	4.38
19	3.95	4.64
20	4.04	4.75
21	4.27	5.01

Table 2-14 • **Bank Wide Delay Values**

	–1	Std.
Bit Setting	**Delay (ns)**	
22	4.38	5.14
23	4.60	5.41
24	4.67	5.49
25	4.90	5.76
26	5.01	5.89
27	5.23	6.15
28	5.32	6.26
29	5.55	6.52
30	5.66	6.65
31	5.88	6.92

Note: *Data for RTAX2000S/SL is shown in the table above; it was measured at V_{CCA} = 1.425 and 125°C.*

Using the Differential I/O Standards

Differential I/O macros should be instantiated in the netlist. The settings for these I/O standards cannot be changed inside Designer. Note that there are no tristated or bidirectional I/O buffers for differential standards.

Using the Voltage-Referenced I/O Standards

Using these I/O standards is similar to that of single-ended I/O standards. Their settings can be changed in Designer.

Using DDR (Double Data Rate)

In Double Data Rate mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

To implement a DDR, users must do the following:

1. Instantiate an input buffer (with the required I/O standard).
2. Instantiate the DDR_REG macro (Figure 2-6).
3. Connect the output from the Input buffer to the input of the DDR macro.
4. DDR supports all I/O standards.
5. The DDR macro in SmartGen can be used to implement DDR.
6. Bit width and I/O standard can be chosen in SmartGen.

Macros for Specific I/O Standards

There are different macro types for any I/O standard or feature that determine the required V_{CCI} and V_{REF} voltages for an I/O. The generic buffer macros require the LVTTL standard with slow slew rate and 24 mA-drive

6. These values are minimum drive strengths.

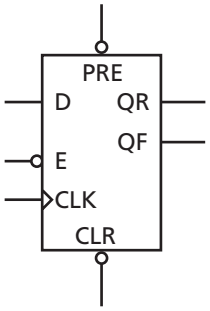


Figure 2-6 • **DDR Register**

strength. LVTTL can support high slew rate but this should only be used for critical signals.

Most of the macro symbols represent variations of the six generic symbol types:

- CLKBUF: Clock Buffer
- HCLKBUF: Hardwired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUFF: Tristate Buffer
- BIBUF: Bidirectional Buffer

Other macros include the following:

- Differential I/O standard macros: The LVDS and LVPECL macros either have a pair of differential inputs (e.g. INBUF_LVDS) or a pair of differential outputs (e.g. OUTBUF_LVPECL).
- Pull-up and pull-down variations of the INBUF, BIBUF, and TRIBUFF macros. These are available only with TTL and LVCMOS thresholds. They can be used to model the behavior of the pull-up and pull-down resistors available in the architecture. Whenever an input pin is left unconnected, the output pin will either go high or low rather than unknown. This allows users to leave inputs unconnected without having the negative effect on simulation of propagating unknowns.
- DDR_REG macro. It can be connected to any I/O standard input buffers (i.e., INBUF) to implement a double data rate register. Designer software will map it to the I/O module in the same way it maps the other registers to the I/O module.

Table 2-15, Table 2-16, and Table 2-17 on page 2-20 list all the available macro names differentiated by I/O standard, type, slew rate, and drive strength.

Table 2-15 • **Macros for Single-Ended I/O Standards**

Standard	V_{CCI}	Macro Names
LVTTL	3.3 V	CLKBUF, HCLKBUF INBUF, OUTBUF, OUTBUF_S_8, OUTBUF_S_12, OUTBUF_S_16, OUTBUF_S_24, OUTBUF_F_8, OUTBUF_F_12, OUTBUF_F_16, OUTBUF_F_24, TRIBUFF, TRIBUFF_S_8, TRIBUFF_S_12, TRIBUFF_S_16, TRIBUFF_S_24, TRIBUFF_F_8, TRIBUFF_F_12, TRIBUFF_F_16, TRIBUFF_F_24, BIBUF, BIBUF_S_8, BIBUF_S_12, BIBUF_S_16, BIBUF_S_24, BIBUF_F_8, BIBUF_F_12, BIBUF_F_16, BIBUF_F_24,
3.3V PCI	3.3 V	CLKBUF_PCI, HCLKBUF_PCI, INBUF_PCI, OUTBUF_PCI, TRIBUFF_PCI, BIBUF_PCI
LVCMOS25	2.5 V	CLKBUF_LVCMOS25, HCLKBUF_LVCMOS25, INBUF_LVCMOS25, OUTBUF_LVCMOS25, TRIBUFF_LVCMOS25, BIBUF_LVCMOS25
LVCMOS18	1.8 V	CLKBUF_LVCMOS18, HCLKBUF_LVCMOS18, INBUF_LVCMOS18, OUTBUF_LVCMOS18, TRIBUFF_LVCMOS18, BIBUF_LVCMOS18
LVCMOS15 (JESD8-11)	1.5 V	CLKBUF_LVCMOS15, HCLKBUF_LVCMOS15, INBUF_LVCMOS15, OUTBUF_LVCMOS15, TRIBUFF_LVCMOS15, BIBUF_LVCMOS15

Table 2-16 • **I/O Macros for Differential I/O Standards**

Standard	V_{CCI}	Macro Names
LVPECL	3.3 V	CLKBUF_LVPECL, HCLKBUF_LVPECL, INBUF_LVPECL, OUTBUF_LVPECL
LVDS	2.5 V	CLKBUF_LVDS, HCLKBUF_LVDS, INBUF_LVDS, OUTBUF_LVDS

Table 2-17 • **I/O Macros for Voltage-Referenced I/O Standards**

Standard	V_{CCI}	V_{REF}	Macro Names
GTL+	3.3 V	1.0 V	CLKBUF_GTP33, HCLKBUF_GTP33, INBUF_GTP33, OUTBUF_GTP33, TRIBUFF_GTP33, BIBUF_GTP33
GTL+	2.5 V	1.0 V	CLKBUF_GTP25, HCLKBUF_GTP25, INBUF_GTP25, OUTBUF_GTP25, TRIBUFF_GTP25, BIBUF_GTP25
SSTL2 Class I	2.5 V	1.25 V	CLKBUF_SSTL2_I, HCLKBUF_SSTL2_I, TRIBUFF_SSTL2_I, BIBUF_SSTL2_I, INBUF_SSTL2_I, OUTBUF_SSTL2_I
SSTL2 Class II	2.5 V	1.25 V	CLKBUF_SSTL2_II, HCLKBUF_SSTL2_II, TRIBUFF_SSTL2_II, BIBUF_SSTL2_II, INBUF_SSTL2_II, OUTBUF_SSTL2_II
SSTL3 Class I	3.3 V	1.5 V	CLKBUF_SSTL3_I, HCLKBUF_SSTL3_I, TRIBUFF_SSTL3_I, BIBUF_SSTL3_I, INBUF_SSTL3_I, OUTBUF_SSTL3_I
SSTL3 Class II	3.3 V	1.5 V	CLKBUF_SSTL3_II, HCLKBUF_SSTL3_II, TRIBUFF_SSTL3_II, BIBUF_SSTL3_II, INBUF_SSTL3_II, OUTBUF_SSTL3_II
HSTL Class I	1.5 V	0.75 V	CLKBUF_HSTL_I, BIBUF_HSTL_I, HCLKBUF_HSTL_I, INBUF_HSTL_I, OUTBUF_HSTL_I, TRIBUFF_HSTL_I

User I/O Naming Conventions

Due to the complex and flexible nature of the RTAX-S/SL family's user I/Os, a naming scheme is used to show the details of the I/O. The naming scheme explains to which bank an I/O belongs, as well as the pairing and pin polarity for differential I/Os (Figure 2-7).

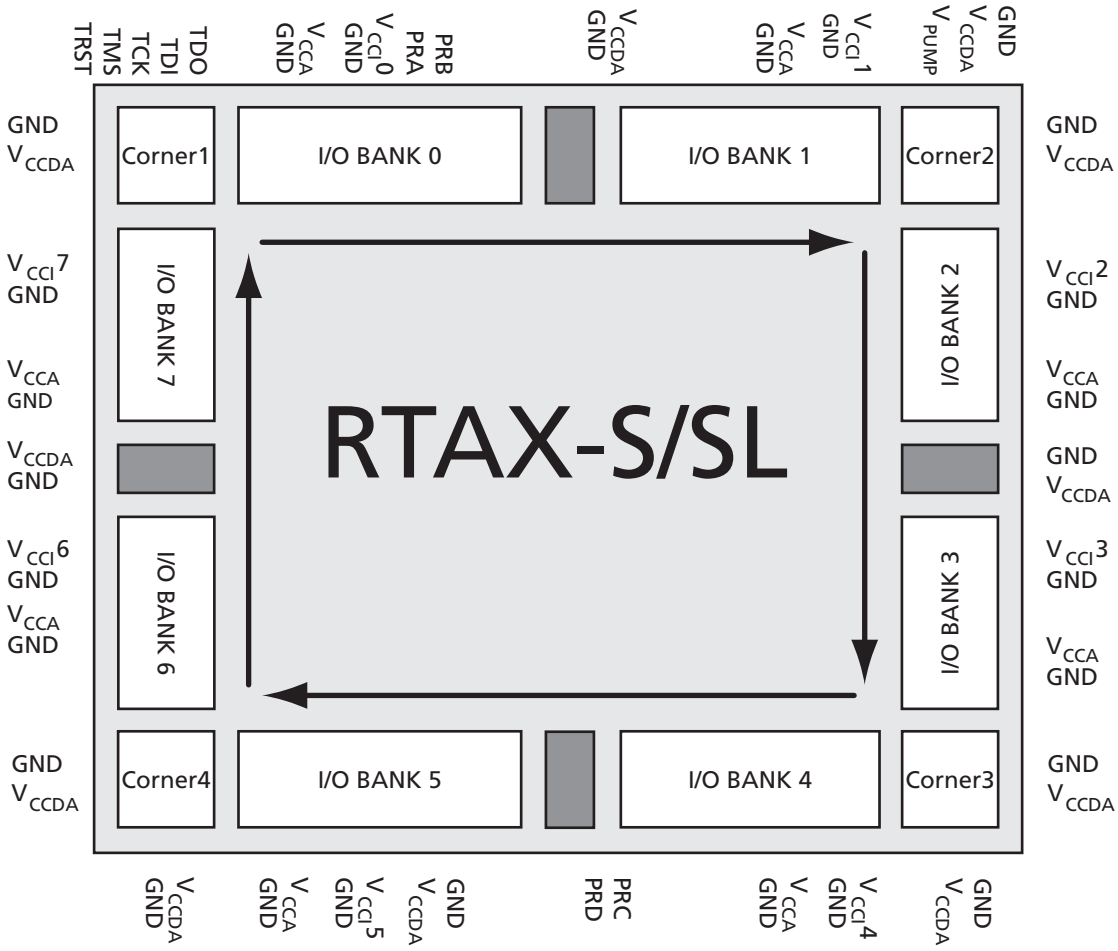
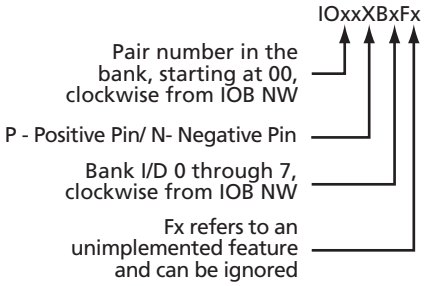


Figure 2-7 • **I/O Bank and Dedicated Pin Layout**



Examples:

IO12PB1F1 Is the positive pin of the thirteenth pair of the first I/O bank (IOB NE). IO12PB1 combined with IO12NB1 form a differential pair.

For those I/Os that can be employed either as a user I/O or as a special function, the following nomenclature is used:

IOxxXBxFx/special_function_name

IOxxPB1Fx/CLKx This pin can be configured as a clock input or as a user I/O

Figure 2-8 • **General Naming Schemes**

I/O Standard Electrical Specifications

Table 2-18 • **Input Capacitance**

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0, f =1.0 MHz		10	pF
C_{INCLK}	Input Capacitance on Clock Pin	V_{IN} = 0, f =1.0 MHz		10	pF

Table 2-19 • **I/O Weak Pull-Up/Pull-Down Resistances**[1]

Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values				
	R(Pull up) (kΩ)[2]		R(Pull down) (kΩ)[3]	
I/O Configuration (V_{CCI})	**Min.**	**Max.**	**Min.**	**Max.**
3.3 V	35	65	30	60
2.5 V	50	75	40	85
1.8 V	80	140	70	130
1.5 V	100	210	90	180

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-20 • **I/O Input Rise Time and Fall Time***

Input Buffer	Input Rise/Fall Time (Min)	Input Rise/Fall Time (Max)
LVTTL	No Requirement	50 ns
LVCMOS 2.5 V	No Requirement	50 ns
LVCMOS 1.8 V	No Requirement	50 ns
LVCMOS 1.5 V	No Requirement	50 ns
PCI	No Requirement	50 ns
PCIX	No Requirement	50 ns
GTL+	No Requirement	50 ns
HSTL	No Requirement	50 ns
SSTL2	No Requirement	50 ns
HSTL3	No Requirement	50 ns
LVDS	No Requirement	50 ns
LVPECL	No Requirement	50 ns

Note: **Input Rise/Fall time applies to all inputs, including clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double-clocking. They must be avoided. For Output Rise/Fall time, refer to IBIS Models for extraction.*

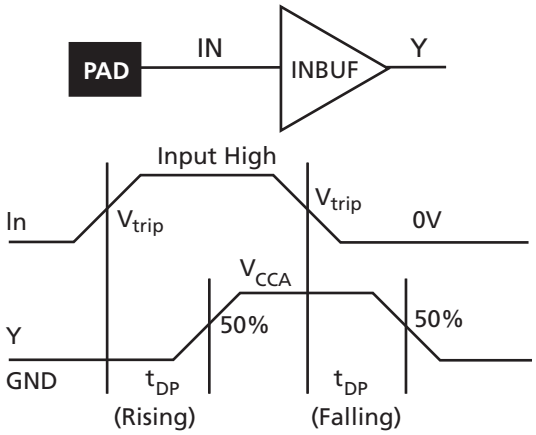


Figure 2-9 • **Input Buffer Delays**

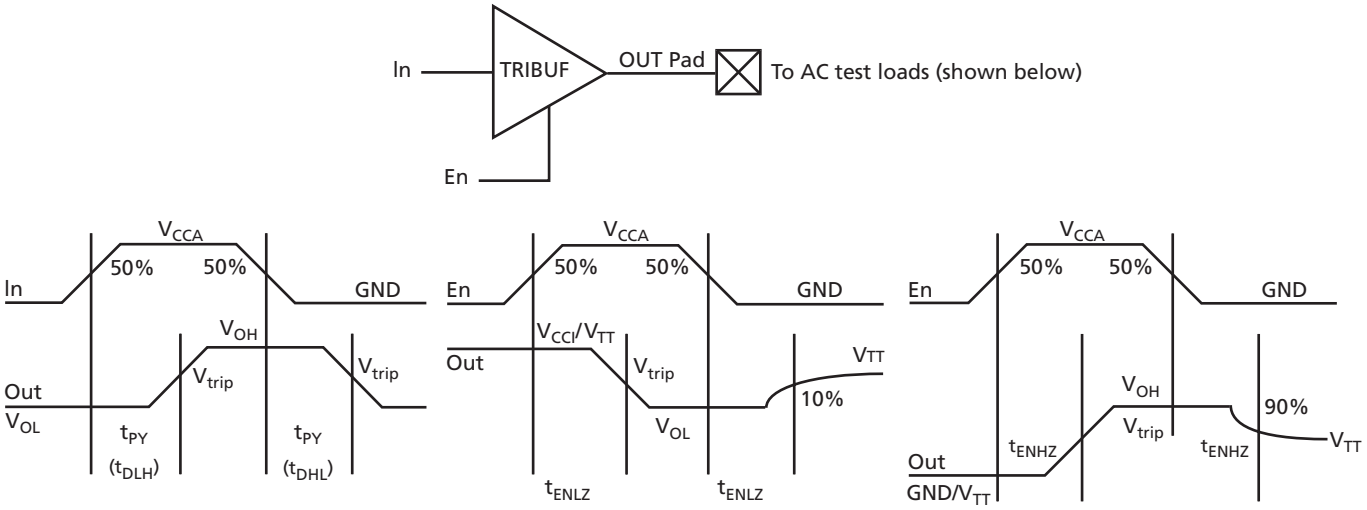


Figure 2-10 • **Output Buffer Delays**

I/O Module Timing Characteristics

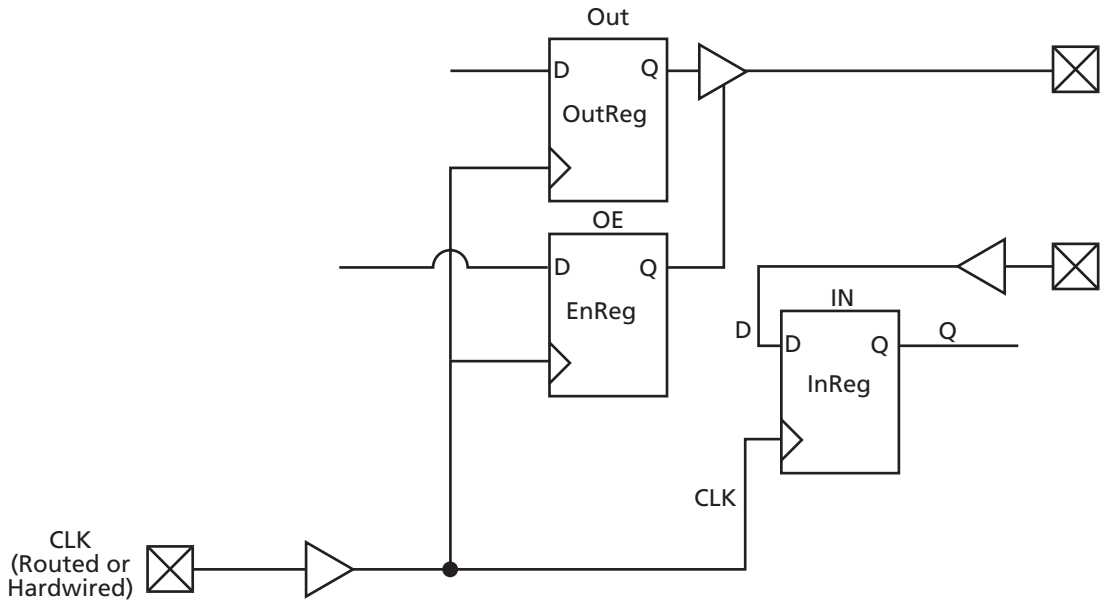


Figure 2-11 • **Timing Model**

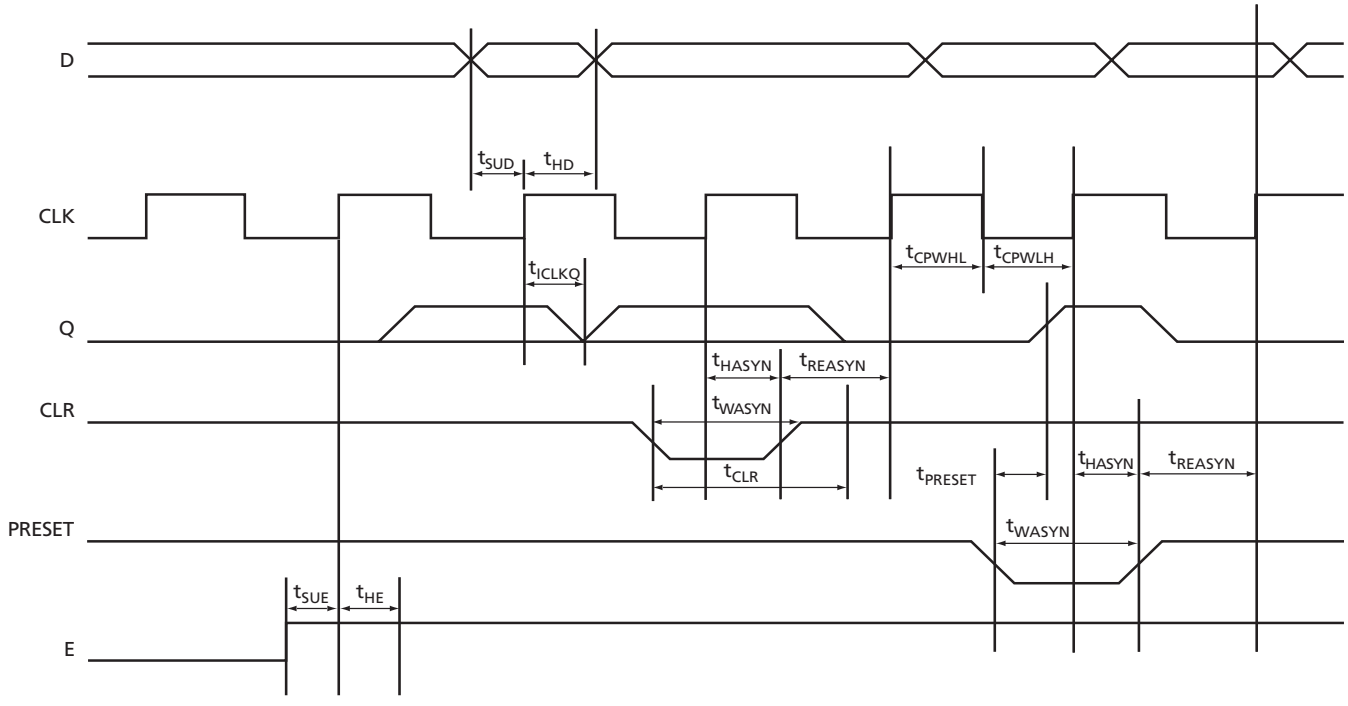


Figure 2-12 • **Input Register Timing Characteristics**

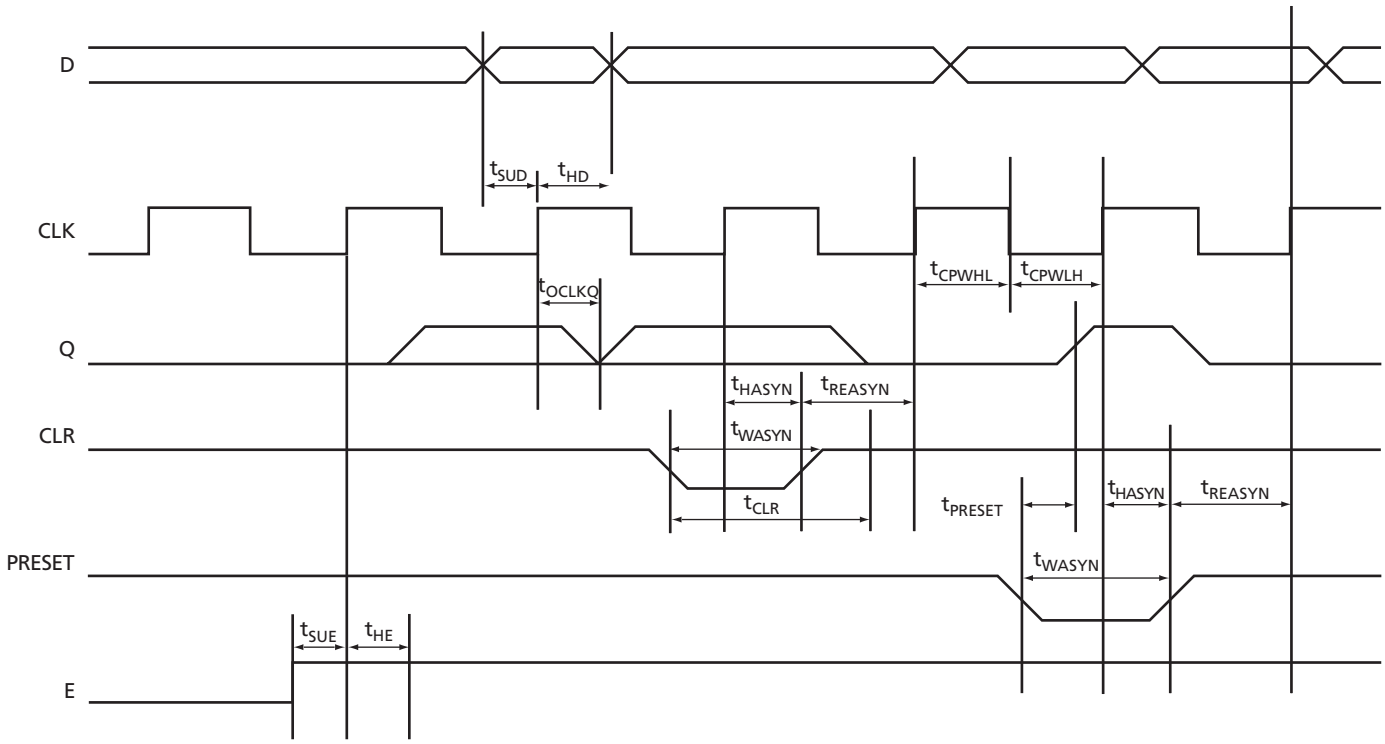


Figure 2-13 • **Output Register Timing Characteristics**

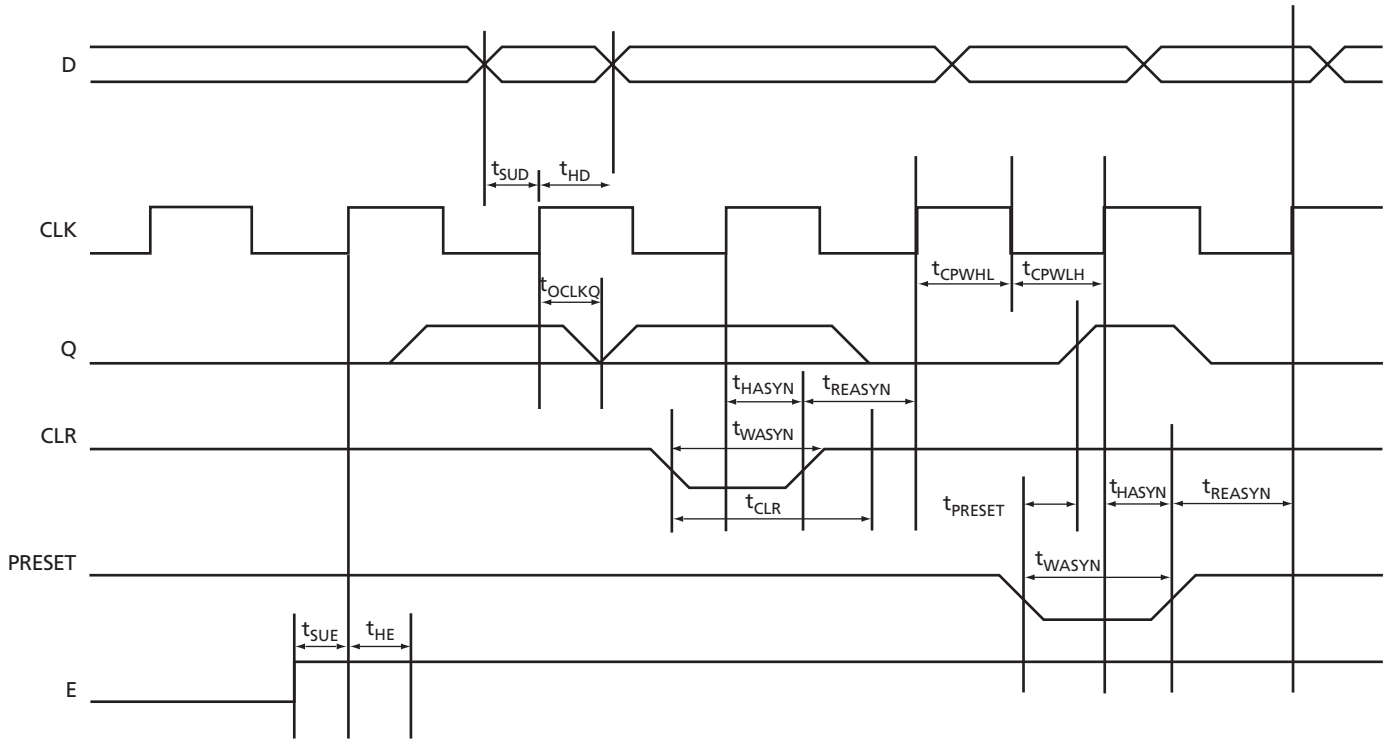


Figure 2-14 • **Output Enable Register Timing Characteristics**

3.3 V LVTTL

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-21 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.3	0.8	2.0	3.6	0.4*	2.4	24	–24

Note: *For RTAX250S/SL-CQ352 devices only, V_{OL} limits are 500 mV across all operating temperatures.*

AC Loadings

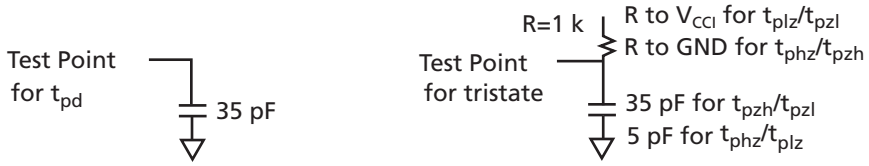


Figure 2-15 • **AC Test Loads**

Table 2-22 • **AC Waveforms, Measuring Points, and Capacitive Load**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**V_{REF} (typ) (V)**	**C_{load} (pF)**
0	3.0	1.40	N/A	35

** Measuring Point = V_{trip}*

Timing Characteristics

Table 2-23 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
LVTTL I/O Module Drive Strength = 1 (8 mA) / Low Slew Rate						
t_{DP}	Input buffer		1.85		2.17	ns
t_{PY}	Output buffer		15.82		18.60	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		16.64		19.56	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		15.56		18.29	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		1.63		1.64	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		1.97		1.97	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 2 (12 mA) / Low Slew Rate						
t_{DP}	Input buffer		1.85		2.17	ns
t_{PY}	Output buffer		13.26		15.58	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		13.56		15.94	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		13.28		15.61	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		1.81		1.82	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		2.24		2.24	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns

Table 2-23 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 3 (16 mA) / Low Slew Rate						
t_{DP}	Input buffer		1.85		2.17	ns
t_{PY}	Output buffer		12.04		14.16	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		12.46		14.65	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		12.05		14.17	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		1.95		1.96	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		2.52		2.53	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 4 (24 mA) / Low Slew Rate						
t_{DP}	Input buffer		1.85		2.17	ns
t_{PY}	Output buffer		11.41		13.41	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		11.58		13.61	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		11.43		13.43	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		2.01		2.02	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		2.59		2.60	ns

Table 2-23 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 1 (8 mA) / High Slew Rate						
t_{DP}	Input buffer		1.85		2.17	ns
t_{PY}	Output buffer		4.78		5.62	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		5.06		5.95	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		4.61		5.42	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		1.98		1.99	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		2.03		2.03	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Table 2-23 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
LVTTL I/O Module Drive Strength = 2 (12 mA) / High Slew Rate						
t_{DP}	Input buffer		1.85		2.17	ns
t_{PY}	Output buffer		3.87		4.55	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		4.08		4.79	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		3.34		3.93	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		1.98		1.99	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		2.31		2.31	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 3 (16 mA) / High Slew Rate						
t_{DP}	Input buffer		1.85		2.17	ns
t_{PY}	Output buffer		3.66		4.31	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		2.47		2.48	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		3.03		3.57	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		2.00		2.01	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		4.07		4.79	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns

Table 2-23 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 4 (24 mA) / High Slew Rate						
t_{DP}	Input buffer		1.85		2.17	ns
t_{PY}	Output buffer		3.51		4.12	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		2.34		2.35	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		1.91		1.92	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		2.96		3.48	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		4.17		4.90	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

2.5 V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-24 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.3	0.7	1.7	3.6	0.4	2.0	12	–12

AC Loadings

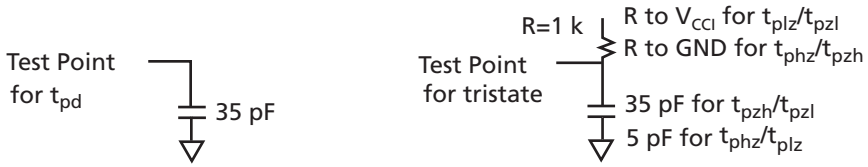


Figure 2-16 • **AC Test Loads**

Table 2-25 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
0	2.5	1.25	N/A	35

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-26 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 2.3 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
LVCMOS25 I/O Module Drive Strength = 1 (6 mA) / Low Slew Rate						
t_{DP}	Input buffer		2.13		2.51	ns
t_{PY}	Output buffer		21.66		25.46	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		22.81		26.81	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		20.47		24.07	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		4.53		4.53	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		4.92		4.92	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low		0.39		0.39	ns
t_{CPWLH}	Clock pulse width Low to High		0.39		0.39	ns
t_{WASYN}	Asynchronous pulse width		0.37		0.37	ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS25 I/O Module Drive Strength = 2 (12 mA) / Low Slew Rate						
t_{DP}	Input buffer		2.13		2.51	ns
t_{PY}	Output buffer		18.09		21.26	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		19.05		22.39	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		17.40		20.46	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		4.53		4.53	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		4.92		4.92	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns

Table 2-26 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 2.3 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS25 I/O Module Drive Strength = 3 (16 mA) / Low Slew Rate						
t_{DP}	Input buffer		2.13		2.51	ns
t_{PY}	Output buffer		16.62		19.53	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		17.50		20.57	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		15.84		18.62	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		4.53		4.53	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		4.92		4.92	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS25 I/O Module Drive Strength = 4 (24 mA) / Low Slew Rate						
t_{DP}	Input buffer		2.13		2.51	ns
t_{PY}	Output buffer		15.66		18.41	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		16.49		19.38	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		15.09		17.74	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		4.53		4.53	ns

Table 2-26 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 2.3 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		4.92		4.92	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS25 I/O Module Drive Strength = 1 (6 mA) / High Slew Rate						
t_{DP}	Input buffer		2.13		2.51	ns
t_{PY}	Output buffer		6.32		7.44	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		3.36		3.37	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		4.26		4.27	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		6.72		7.90	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		7.72		9.08	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Table 2-26 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 2.3 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
LVCMOS25 I/O Module Drive Strength = 2 (12 mA) / High Slew Rate						
t_{DP}	Input buffer		2.13		2.51	ns
t_{PY}	Output buffer		4.43		5.21	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		2.61		2.62	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		2.99		3.00	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		6.72		7.90	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		7.72		9.08	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS25 I/O Module Drive Strength = 3 (16 mA) / High Slew Rate						
t_{DP}	Input buffer		2.13		2.51	ns
t_{PY}	Output buffer		3.91		4.59	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		2.46		2.47	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		2.64		2.64	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		6.72		7.90	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		7.72		9.08	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns

Table 2-26 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 2.3 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS25 I/O Module Drive Strength = 4 (24 mA) / High Slew Rate						
t_{DP}	Input buffer		2.13		2.51	ns
t_{PY}	Output buffer		3.59		4.22	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		2.34		2.35	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		2.43		2.43	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		6.72		7.90	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		7.72		9.08	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

1.8 V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-27 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.3	$0.2V_{CCI}$	$0.7V_{CCI}$	2.1	0.2	V_{CCI}-0.2	8mA	–8mA

AC Loadings

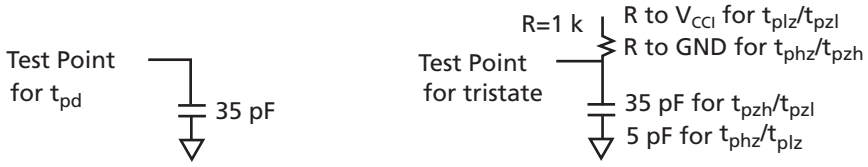


Figure 2-17 • **AC Test Loads**

Table 2-28 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**V_{REF} (typ) (V)**	**C_{load} (pF)**
0	1.8	$0.5V_{CCI}$	N/A	35

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-29 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.7 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
LVCMOS18 I/O Module Drive Strength = 2 (2 mA) / Low Slew Rate						
t_{DP}	Input buffer		3.57		4.19	ns
t_{PY}	Output buffer		33.79		39.72	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		35.58		41.83	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		26.65		31.33	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		4.74		4.75	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		5.02		5.02	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS18 I/O Module Drive Strength = 3 (6 mA) / Low Slew Rate						
t_{DP}	Input buffer		3.57		4.19	ns
t_{PY}	Output buffer		31.06		36.51	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		32.70		38.44	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		24.32		28.59	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		4.74		4.75	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		5.02		5.02	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns

Table 2-29 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.7 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS18 I/O Module Drive Strength = 4 (8 mA) / Low Slew Rate						
t_{DP}	Input buffer		3.57		4.19	ns
t_{PY}	Output buffer		29.73		34.95	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		31.31		36.80	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		23.23		27.31	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		4.74		4.75	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		5.02		5.02	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS18 I/O Module Drive Strength = 2 (2 mA) / High Slew Rate						
t_{DP}	Input buffer		3.57		4.19	ns
t_{PY}	Output buffer		6.54		7.69	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		3.06		3.07	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		4.41		4.41	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		7.04		8.27	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		7.88		9.26	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns

Table 2-29 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.7 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS18 I/O Module Drive Strength = 3 (6 mA) / High Slew Rate						
t_{DP}	Input buffer		3.57		4.19	ns
t_{PY}	Output buffer		5.55		6.52	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		2.85		2.86	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		3.74		3.75	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		7.04		8.27	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		7.88		9.26	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Table 2-29 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.7 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
LVCMOS18 I/O Module Drive Strength = 4 (8 mA) / High Slew Rate						
t_{DP}	Input buffer		4.97		5.85	ns
t_{PY}	Output buffer		2.65		2.66	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		3.35		3.36	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		7.04		8.27	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		7.88		9.26	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		0.91		1.07	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.31		0.37	ns
t_{SUD}	Data input setup		0.35		0.41	ns
t_{SUE}	Enable input setup		0.00		0.00	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold	0.39		0.39		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width		0.17		0.21	ns
t_{REASYN}	Asynchronous recovery time		0.00		0.00	ns
t_{HASYN}	Asynchronous removal time		0.31		0.37	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		4.97		5.85	ns

1.5 V LVCMOS (JESD8-11)

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 3.3 V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-30 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.5	$0.35V_{CCI}$	$0.65V_{CCI}$	1.95	0.4	V_{CCI}-0.4	8mA	–8mA

AC Loadings

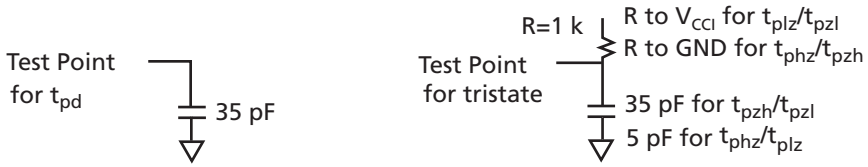


Figure 2-18 • **AC Test Loads**

Table 2-31 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
0	1.5	$0.5V_{CCI}$	N/A	35

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-32 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.4 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
LVCMOS15 I/O Module Drive Strength = 1 (2 mA) / Low Slew Rate						
t_{DP}	Input buffer		3.93		4.62	ns
t_{PY}	Output buffer		60.38		70.98	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		63.58		74.74	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		44.80		52.67	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		5.02		5.02	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		5.17		5.17	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS15 I/O Module Drive Strength = 2 (4 mA) / Low Slew Rate						
t_{DP}	Input buffer		3.93		4.62	ns
t_{PY}	Output buffer		53.29		62.65	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		56.12		65.97	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		37.88		44.53	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		5.02		5.02	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		5.17		5.17	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns

Table 2-32 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.4 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS15 I/O Module Drive Strength = 3 (6 mA) / Low Slew Rate						
t_{DP}	Input buffer		3.93		4.62	ns
t_{PY}	Output buffer		48.90		57.49	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		51.50		60.54	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		34.84		40.95	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		5.02		5.02	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		5.17		5.17	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS15 I/O Module Drive Strength = 8 (4 mA) / Low Slew Rate						
t_{DP}	Input buffer		3.93		4.62	ns
t_{PY}	Output buffer		47.21		55.49	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		49.71		58.43	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		33.18		39.01	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		5.02		5.02	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		5.17		5.17	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns

Table 2-32 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.4 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS15 I/O Module Drive Strength = 1 (2 mA) / High Slew Rate						
t_{DP}	Input buffer		3.93		4.62	ns
t_{PY}	Output buffer		14.59		17.15	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		8.38		9.85	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		14.59		17.15	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		5.02		5.02	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		5.17		5.17	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS15 I/O Module Drive Strength = 2 (4 mA) / High Slew Rate						
t_{DP}	Input buffer		3.93		4.62	ns

Table 2-32 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.4 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{PY}	Output buffer		9.12		10.73	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		3.69		3.70	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		9.12		10.73	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		5.02		5.02	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		8.12		9.54	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS15 I/O Module Drive Strength = 3 (6 mA) / High Slew Rate						
t_{DP}	Input buffer		3.93		4.62	ns
t_{PY}	Output buffer		7.62		8.96	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		3.42		3.42	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		7.62		8.96	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		5.02		5.02	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		8.12		9.54	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns

Table 2-32 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.4 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVCMOS15 I/O Module Drive Strength = 4 (8 mA) / High Slew Rate						
t_{DP}	Input buffer		3.93		4.62	ns
t_{PY}	Output buffer		6.60		7.76	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		3.12		3.13	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		4.45		4.46	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		7.45		8.76	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		8.12		9.54	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

3.3 V PCI

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. The input and output buffers are 5V tolerant with the aid of external components. The RTAX-S/SL 3.3 V PCI buffer is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-33 • **DC Input and Output Levels**

	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
PCI	–0.5	$0.3V_{CCI}$	$0.5V_{CCI}$	V_{CCI}+0.5	(per PCI specification)			

AC Loadings

Per PCI Specification except for tristate. Actel loading for tristate is in the figure below.

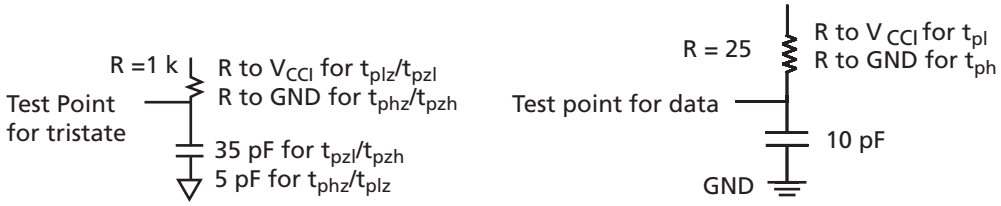


Figure 2-19 • **AC Test Loads**

Table 2-34 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**V_{REF} (typ) (V)**	**C_{load} (pF)**
(Per PCI Spec)			N/A	10

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-35 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
3.3V PCI I/O Module Timing						
t_{DP}	Input buffer		1.72		2.02	ns
t_{PY}	Output buffer		2.25		2.64	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		1.52		1.52	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		1.42		1.43	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		2.98		3.50	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		4.12		4.84	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Table 2-36 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
3.3V PCI-X I/O Module Timing						
t_{DP}	Input buffer		1.72		2.02	ns
t_{PY}	Output buffer		2.30		2.71	ns
t_{ENZL}	Enable to Pad delay through the Output Buffer—HIGH to Z		1.52		1.52	ns
t_{ENZH}	Enable to Pad delay through the Output Buffer—Z to HIGH		1.56		1.57	ns
t_{ENLZ}	Enable to Pad delay through the Output Buffer—LOW to Z		3.10		3.65	ns
t_{ENHZ}	Enable to Pad delay through the Output Buffer—Z to LOW		3.64		4.28	ns
t_{IOCLKQ}	Sequential clock-to-Q for the input register		0.91		1.07	ns
t_{IOCLKY}	Clock-to-output Y for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Voltage-Referenced I/O Standards

GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It requires a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 2.5 V or 3.3 V. Note that 2.5 V GTL+ is not supported across the full military temperature range.

Table 2-37 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
N/A	V_{REF}-0.1	V_{REF}+0.1	N/A	0.6*	NA	NA	NA

Note: *For high temperature of 125°C only, V_{OL} limits are 700 mV, for all other temperatures 600 mV applies.*

AC Loadings

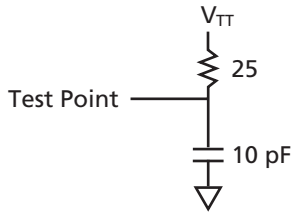


Figure 2-20 • **AC Test Loads**

Table 2-38 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-0.2	V_{REF}+0.2	V_{REF}	1.0	10

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-39 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
3.3 V GTL+ I/O Module Timing						
t_{DP}	Input buffer		2.01		2.36	ns
t_{PY}	Output buffer		1.26		1.49	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). The RTAX-S/SL devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

Table 2-40 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CC}-0.4	8	–8

AC Loadings

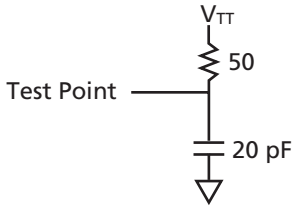


Figure 2-21 • **AC Test Loads**

Table 2-41 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-0.5	V_{REF}+0.5	V_{REF}	0.75	20

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-42 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 1.4 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
1.5 V HSTL Class I I/O Module Timing						
t_{DP}	Input buffer		2.12		2.49	ns
t_{PY}	Output buffer		5.35		6.29	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

SSTL2

Stub Series Terminated Logic for 2.5 V is a general-purpose 2.5 V memory bus standard (JESD8-9). The RTAX-S/SL devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-43 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.57	V_{REF}+0.57	7.6	–7.6

AC Loadings

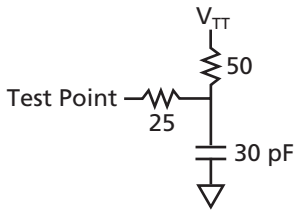


Figure 2-22 • **AC Test Loads**

Table 2-44 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-0.75	V_{REF}+0.75	V_{REF}	1.25	30

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-45 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 2.3 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
2.5 V SSTL2 Class I I/O Module Timing						
t_{DP}	Input buffer		2.14		2.52	ns
t_{PY}	Output buffer		2.61		3.07	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Class II

Table 2-46 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.8	V_{REF}+0.8	15.2	–15.2

AC Loadings

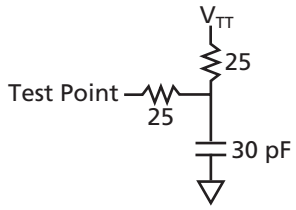


Figure 2-23 • **AC Test Loads**

Table 2-47 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-0.75	V_{REF}+0.75	V_{REF}	1.25	30

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-48 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 2.3 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
2.5 V SSTL2 Class II I/O Module Timing						
t_{DP}	Input buffer		2.22		2.61	ns
t_{PY}	Output buffer		2.61		3.07	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

SSTL3

Stub Series Terminated Logic for 3.3 V is a general-purpose 3.3 V memory bus standard (JESD8-8). The RTAX-S/SL devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-49 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.6	V_{REF}+0.6	8	–8

AC Loadings

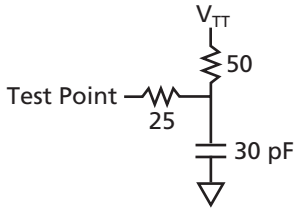


Figure 2-24 • **AC Test Loads**

Table 2-50 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-1.0	V_{REF}+1.0	V_{REF}	1.50	30

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-51 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
3.3 V SSTL3 Class I I/O Module Timing						
t_{DP}	Input buffer		2.09		2.46	ns
t_{PY}	Output buffer		2.55		2.99	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Class II

Table 2-52 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
–0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.8	V_{REF}+0.8	16	–16

AC Loadings

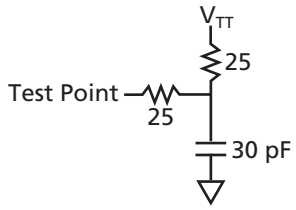


Figure 2-25 • **AC Test Loads**

Table 2-53 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-1.0	V_{REF}+1.0	V_{REF}	1.50	30

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-54 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
3.3 V SSTL3 Class II I/O Module Timing						
t_{DP}	Input buffer		2.17		2.55	ns
t_{PY}	Output buffer		2.55		2.99	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Differential Standards

Physical Implementation

Implementing differential I/O standards requires the configuration of a pair of external I/O pads, resulting in a single internal signal. To facilitate construction of the differential pair, a single I/O cluster contains the resources for a pair of I/Os. Configuration of the I/O Cluster as a differential pair is handled by Actel's Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), and Enable Register (EnReg). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit is carried through two signal lines, so two pins are needed. It also requires an external resistor termination. The voltage swing between these two signal lines is approximately 350 mV.

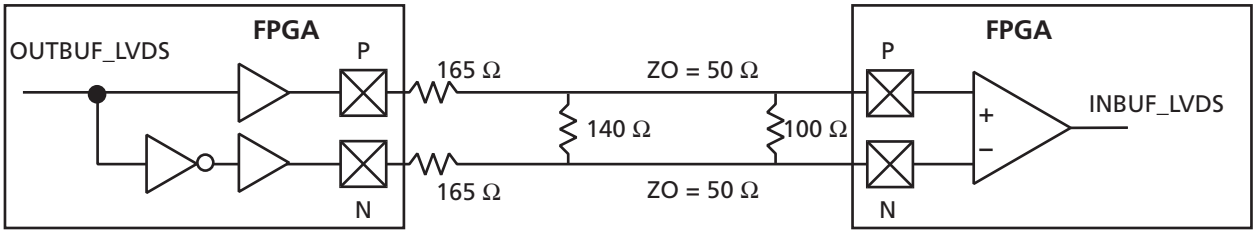


Figure 2-26 • **LVDS Circuit**

The LVDS circuit consists of a differential driver connected to a terminated receiver through a constant-impedance transmission line. The receiver is a wide-common-mode-range differential amplifier. The common-mode range is from 0.2 V to 2.2 V for a differential input with 400 mV swing.

To implement the driver for the LVDS circuit, drivers from two adjacent I/O cells are used to generate the differential signals (Note that the driver is not a current-mode driver). This driver provides a nominal constant current of 3.5 mA. When this current flows through a 100 Ω termination resistor on the receiver side, a voltage swing of 350 mV is developed across the resistor. The direction of the current flow is controlled by the data fed to the driver.

An external-resistor network (three resistors) is needed to reduce the voltage swing to about 350 mV. Therefore, four external resistors are required, three for the driver and one for the receiver.

Table 2-55 • **DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}[1]	Supply voltage	2.375	2.5	2.625	V
V_{OL}	Output low voltage	0.9	1.075	1.25	V
V_{OH}	Output high voltage	1.25	1.425	1.6	V
V_I	Input voltage	0		2.925	V
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}[2]	Input common mode voltage	0.2	1.25	2.2	V
V_{IDIFF}	Differential input voltage	100	350		mV

Notes:

1. *+/- 5%*
2. *Differential input voltage = ±400 mV.*

AC Loadings

For AC test loads, see the above LVDS circuit.

Table 2-56 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{load} (pF)
1.2-0.125	1.2+0.125	1.2	N/A

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-57 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 2.3 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVDS I/O Module Timing						
t_{DP}	Input buffer		2.00		2.35	ns
t_{PY}	Output buffer		2.54		2.99	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination. The voltage swing between these two signal lines is approximately 850 mV.

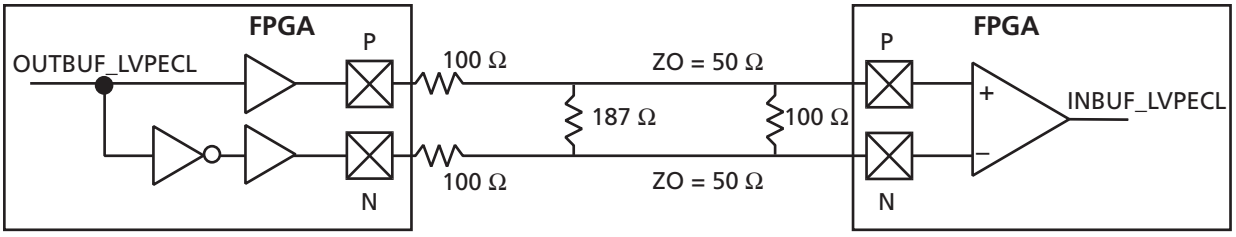


Figure 2-27 • **LVPECL Circuit**

The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS, since the output voltage levels are different. Please note that the V_{OH} levels are 200 mV below the standard LVPECL levels.

Table 2-58 • **DC Input and Output Levels**

	Min.		Typ.		Max.		
DC Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCI}	3	–	3.3	–	3.6	–	V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

AC Loadings

For AC test loads, See the above LVPECL circuit.

Table 2-59 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{load} (pF)
1.6-0.3	1.6+0.3	1.6	N/A

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-60 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVPECL I/O Module Timing						
t_{DP}	Input buffer		1.83		2.15	ns
t_{PY}	Output buffer		2.45		2.88	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup		0.31		0.37	ns
t_{SUE}	Enable input setup		0.35		0.41	ns
t_{HD}	Data input hold		0.00		0.00	ns
t_{HE}	Enable input hold		0.00		0.00	ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.39		0.39		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time		0.17		0.21	ns
t_{HASYN}	Asynchronous removal time		0.00		0.00	ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Module Specifications

C-Cell

Introduction

The C-cell is one of the two logic module types in the RTAX-S/SL architecture. It is the combinatorial logic resource in the RTAX-S/SL device. The RTAX-S/SL architecture implements a new Combinatorial Cell that is an extension of the C-cell implemented in the A54SX-A family. The main enhancement of the new C-cell is the addition of carry-chain logic.

The C-cell can be used in a carry-chain mode to construct arithmetic functions. If carry-chain logic is not required, it can be disabled.

The C-cell features the following (Figure 2-28):

- Eight-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. Any of the C-cell inputs (D0-D3, A0, A1, B0, B1) can be tied to one of the four routed clocks (CLKE/F/G/H).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell.
- A carry input and a carry output. The carry input signal of the C-cell is the carry output from the C-cell directly to the north.
- Carry connect for carry-chain logic with a signal propagation time of less than 0.1 ns.
- A hardwired connection (direct connect) to the adjacent R-cell (Register Cell) for all C-cells on the east side of a SuperCluster with a signal propagation time of less than 0.1 ns.

This layout of the C-cell (and the C-cell Cluster) enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a four-input XOR function in a single cell delay.

The carry-chain configuration is handled automatically for the user with the extensive Actel macro library. Refer to the Actel *Antifuse Macro Library Guide* for a complete listing of available RTAX-S/SL macros.

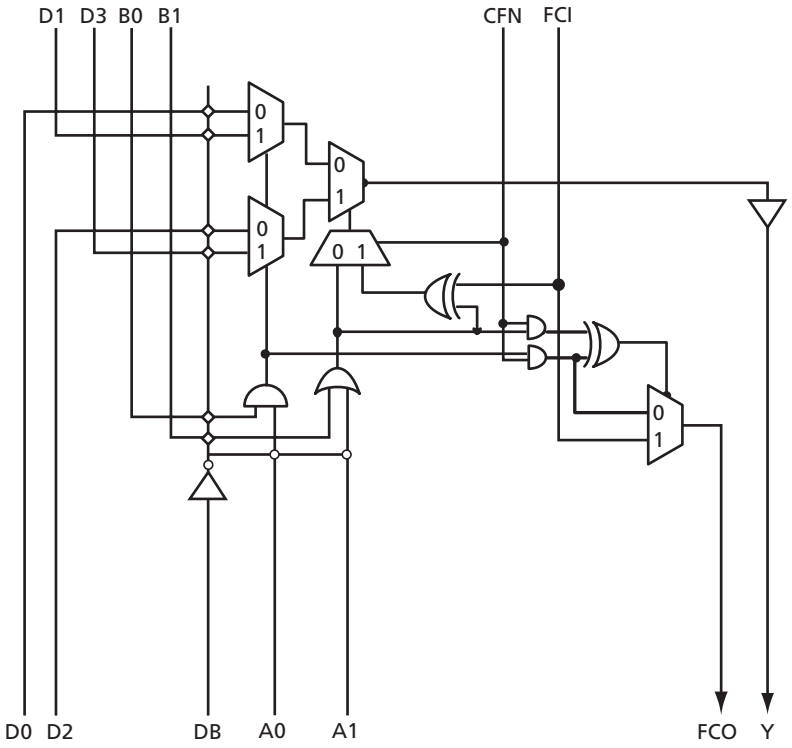


Figure 2-28 • **C-Cell**

Timing Model and Waveforms

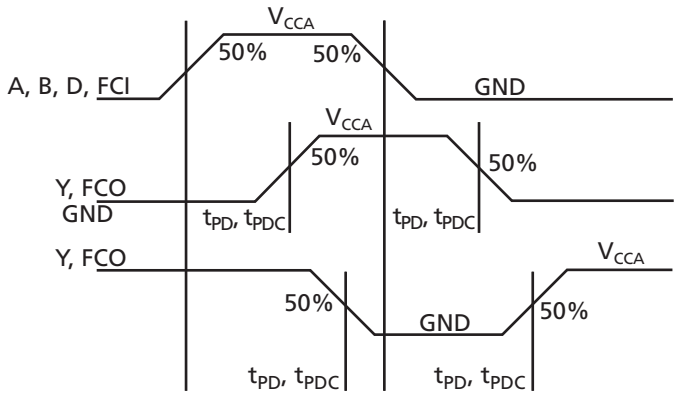


Figure 2-29 • **C-Cell Timing Model and Waveforms**

Timing Characteristics

Table 2-61 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
C-Cell Propagation Delays						
t_{PD}	Any input to output		0.95		1.11	ns
t_{PDC}	Any input to carry chain output (FCO)		0.70		0.82	ns
t_{PDB}	Any input thorough DB when 1 input is used		1.49		1.75	ns
t_{CCY}	Input carry chain (FCI) to Y		0.76		0.90	ns
t_{CC}	Input carry chain (FCI) to carry chain output (FCO)		0.10		0.12	ns

Carry-Chain Logic

The RTAX-S/SL dedicated carry-chain logic offers a very compact solution for implementing arithmetic functions without sacrificing performance.

To implement the carry-chain logic, two C-cells in a Cluster are connected together so the FCO (i.e., carry out) for the two bits is generated in a Carry Look-ahead scheme to achieve minimum propagation delay from the FCI (i.e., carry in) into the two-bit Cluster. The two-bit carry logic is shown in Figure 2-30.

The FCI of one C-cell pair is driven by the FCO of the C-cell pair immediately above it. Similarly, the FCO of one C-cell pair, drives the FCI input of the C-cell pair immediately below it (Figure 1-5 on page 1-3 and Figure 2-31 on page 2-65).

The carry-chain logic is selected via the CFN input. When carry logic is not required, this signal is deasserted to save power. Again, this configuration is handled automatically for the user through the Actel macro library.

The signal propagation delay between two C-cells in the carry-chain sequence is 0.1 ns.

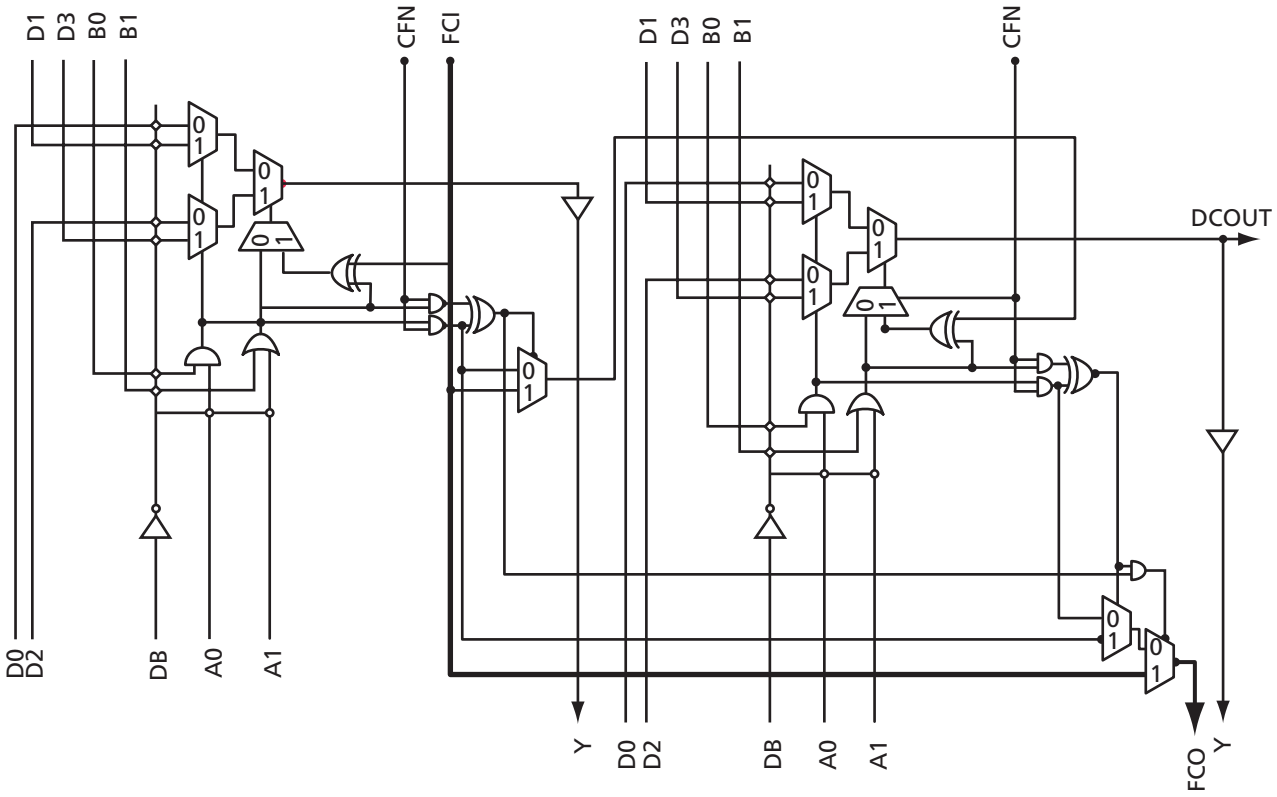
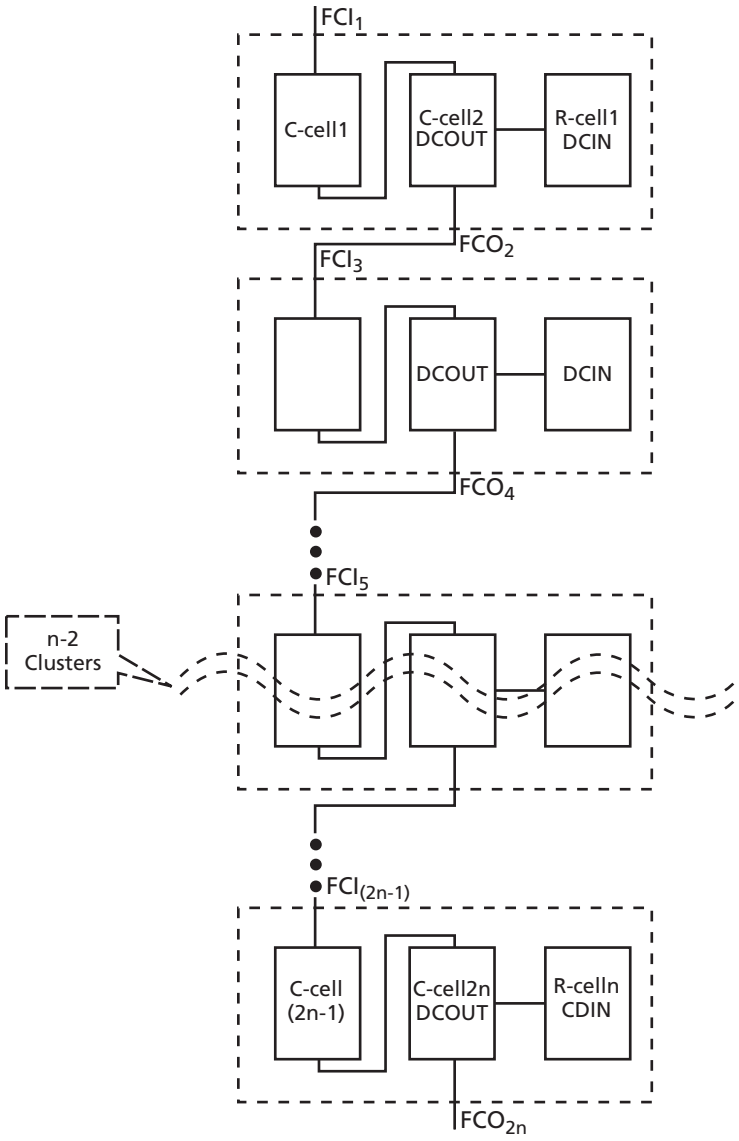


Figure 2-30 • **RTAX-S/SL Two-Bit Carry Logic**



Note: *The carry-chain sequence can end on either C-cell.*

Figure 2-31 • **Carry-Chain Sequencing of C-Cells**

Timing Characteristics

Refer to the C-cell timing characteristics in Table 2-61 on page 2-63 for more information on carry-chain timing.

R-Cell

Introduction

The R-cell, the sequential logic resource of the RTAX-S/SL devices, is the second logic module type in the RTAX-S/SL family architecture. The RTAX-S/SL R-cell is an enhanced version of the A54SX-A R-cell. It includes additional clock inputs for all eight global resources of the RTAX-S/SL architecture as well as global presets and clears (Figure 2-32).

The main features of the R-cell include the following:

- Direct connection to the adjacent logic module through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1 ns of routing delay.
- The R-cell can be used as a standalone flip-flop. It can be driven by any C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using the R-cell as a 2:1 MUXed flip-flop as well.
- Provision of data enable-input (S0).
- Independent active low asynchronous clear (CLR).
- Independent active low asynchronous preset (PSET). If both CLR and PSET are low, CLR has higher priority.
- Clock can be driven by any of the following (CKP selects clock polarity):
  - One of the four high performance hardwired fast clocks (HCLKs)
  - One of the four routed clocks (CLKs)
  - User signals
- Global power-on clear (GCLR) and preset (GPSET), which drive each flip-flop on a chip-wide basis.
  - When the Global Set Fuse option in the Designer software is unchecked (by default), GCLR = 0 and GPSET =1 at device power-up. When the option is checked, GCLR = 1 and GPSET= 0. Both pins are pulled HIGH when the device is in user mode.
- S0, S1, PSET, and CLR can be driven by routed clocks CLKE/F/G/H or user signals.
- DIN and S1 can be driven by user signals.

As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Actel's extensive macro library (please see the Actel *Macro Library Guide* for a complete listing of available RTAX-S/SL macros).

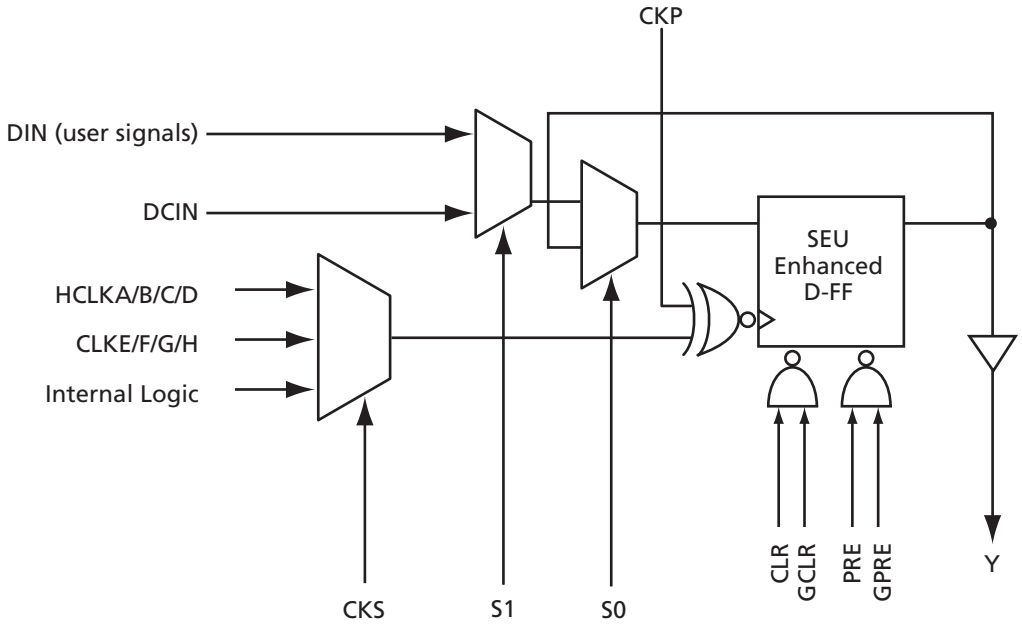


Figure 2-32 • **R-Cell**

SEU Hardened D Flip-Flop (DFF)

In order to meet the stringent SEU requirements of a LET_{TH} greater than 37 MeV-cm^2/mg, the internal design of the R-cell was modified without changing the functionality of the cell. Figure 2-33 illustrates a simplified representation of how the D flip-flop in the SuperCluster is implemented in the RTAX-S/SL architecture. The flip-flop consists of a master and a slave latch gated by opposite edges of the clock. Each latch is constructed by feeding back the output to the input stage. The potential problem in a space environment is that either of the latches can change state when hit by a particle with enough energy.

To achieve the SEU requirements, the D flip-flop in the RTAX-S/SL R-cell is enhanced (Figure 2-34). Both the master and slave "latches" are actually implemented with three latches. The asynchronous self-correcting feedback paths of each of the three latches is voted with the outputs of the other two latches. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching. Care was taken in the layout to ensure that a single ion strike could not affect more than one latch. Figure 2-35 on page 2-68 is a simplified schematic of the test circuitry that has been added to test the functionality of all the components of the flip-flop. The inputs to each of the three latches are independently controllable, so the voting circuitry in the asynchronous self-correcting feedback paths can be tested exhaustively. This testing is performed on an unprogrammed array during wafer sort, final test, and post-burn-in test. This test circuitry cannot be used to test the flip-flops once the device has been programmed.

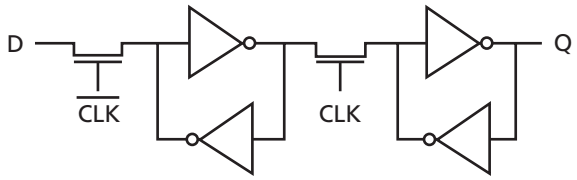


Figure 2-33 • **RTAX-S/SL R-cell Implementation of D Flip-Flop**

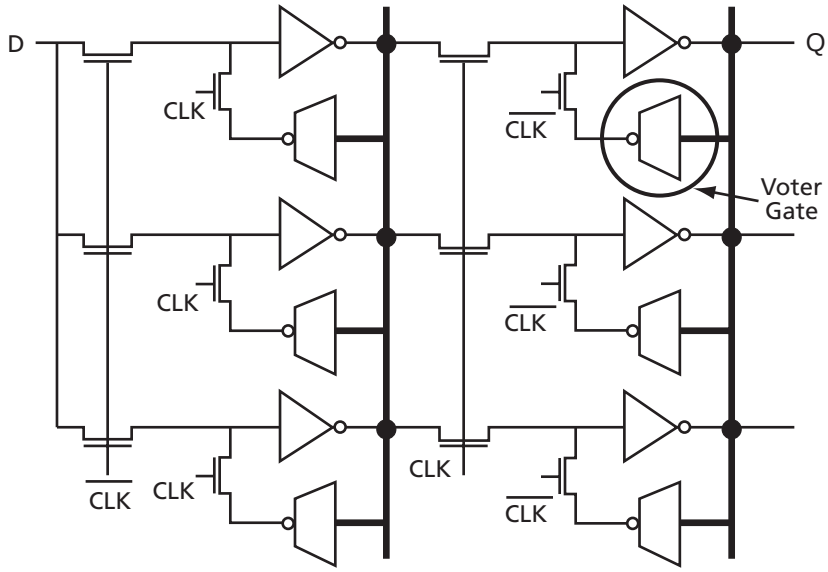


Figure 2-34 • **RTAX-S/SL R-cell Implementation of D Flip-Flop Using Voter Gate Logic**

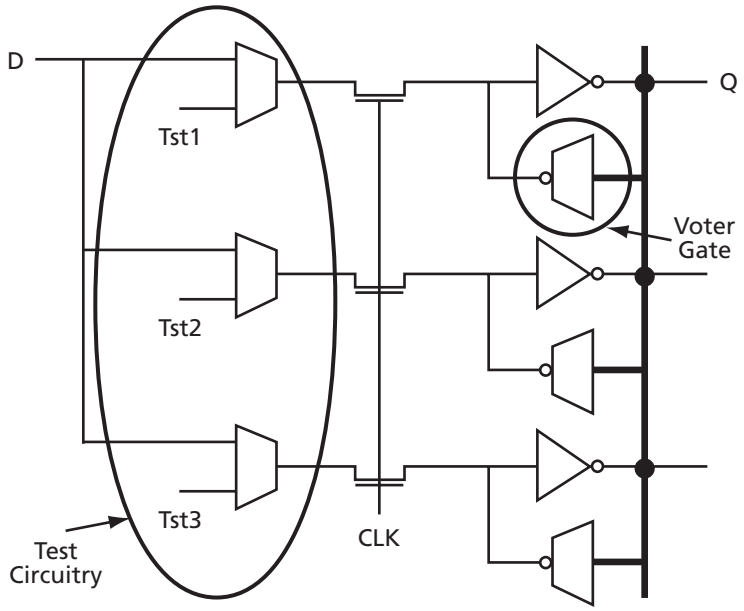


Figure 2-35 • **RTAX-S/SL R-Cell Implementation – Test Circuitry**

Timing Models and Waveforms

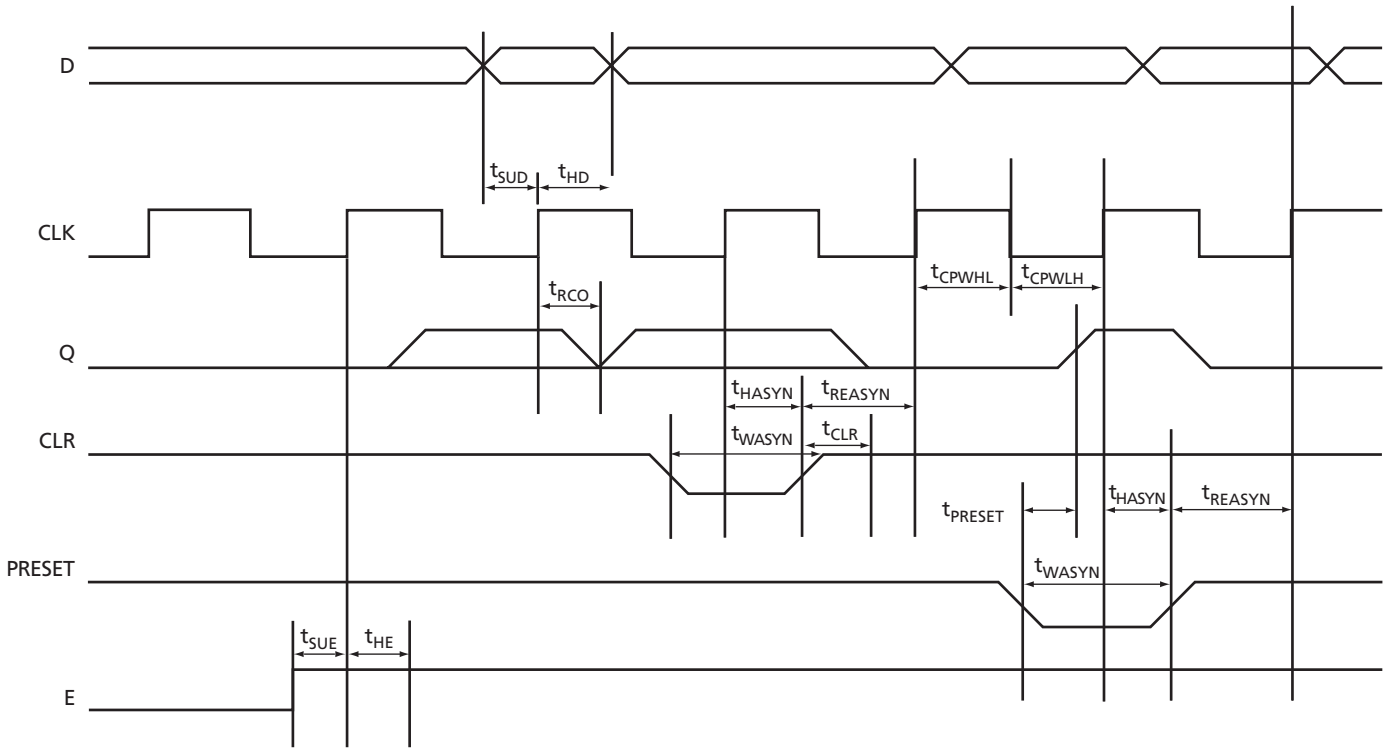


Figure 2-36 • **R-Cell Delays**

Timing Characteristics

Table 2-62 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
R-Cell Propagation Delays						
t_{RCO}	Sequential Clock to Q		0.96		1.12	ns
t_{CLR}	Asynchronous Clear to Q		0.63		0.74	ns
t_{PRESET}	Asynchronous Preset to Q		0.76		0.89	ns
t_{SUD}	FF Data input setup	0.21		0.25		ns
t_{SUE}	FF Enable input setup	0.21		0.25		ns
t_{HD}	FF Data Hold	0.00		0.00		ns
t_{HE}	FF Enable Hold time	0.00		0.00		ns
t_{WASYN}	Asynchronous Pulse width	0.48		0.48		ns
t_{REASYN}	Asynchronous Recovery time	0.00		0.00		ns
t_{HASYN}	Asynchronous Removal time	0.00		0.00		ns
t_{CPWHL}	Clock pulse width high to low	0.36		0.36		ns
t_{CPWLH}	Clock pulse width low to high	0.36		0.36		ns

Buffer Module

Introduction

An additional resource inside each SuperCluster is the Buffer (B) module (Figure 1-4 on page 1-3).

When a fanout constraint is applied to a design, the synthesis tool inserts buffers as needed. The buffer module has been added to the RTAX-S/SL architecture to avoid logic duplication resulting from the hard fanout constraints. The router utilizes this logic resource to save area and reduce loading and delays on medium-to-high-fanout nets.

Timing Models and Waveforms

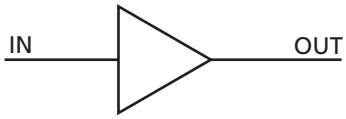


Figure 2-37 • **Buffer Module Timing Model**

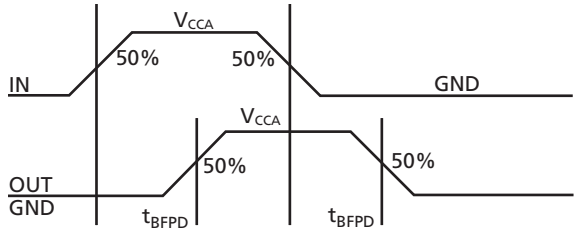


Figure 2-38 • **Buffer Module Waveform**

Timing Characteristics

Table 2-63 • **Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{BFPD}	Any input to output Y		0.17		0.20	ns

Routing Specifications

Routing Resources

The routing structure found in RTAX-S/SL devices enables any logic module to be connected to any other logic module while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

There are four primary types of routing within the RTAX-S/SL architecture: DirectConnect, CarryConnect, FastConnect and Vertical and Horizontal Routing.

DirectConnect

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (Figure 2-39). This connection can be made from DCOUT of the C-cell to DCIN of the R-cell by configuring of the S1 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.

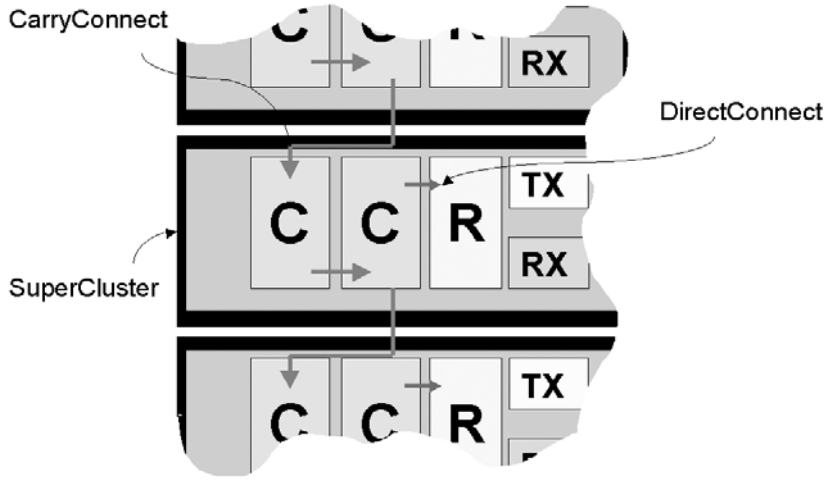


Figure 2-39 • **DirectConnect and CarryConnect**

CarryConnect

CarryConnects are used to build carry chains for arithmetic functions (Figure 2-39). The FCO output of the right C-cell of a two-C-cell Cluster drives the FCI input of the left C-cell in the two-C-cell Cluster immediately below it. This pattern continues down both sides of each SuperCluster column.

Similar to the DirectConnects, CarryConnects can be built without an antifuse connection. This connection has a delay of less than 0.1 ns from the FCO of one two-C-cell Cluster to the FCI of the two-C-cell Cluster immediately below it (see the "Carry-Chain Logic" on page 2-64 for more information).

FastConnect

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (Figure 2-40 on page 2-71). FastConnects provide a maximum delay of 0.4 ns. The outputs of each logic module connect directly to the Output Tracks within a SuperCluster. Signals on the Output Tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below it.

Vertical and Horizontal Routing

Vertical and Horizontal Tracks provide both local and long distance routing (Figure 2-41 on page 2-71). These tracks are composed of both short-distance, segmented routing and across-chip routing tracks (segmented at core tile boundaries). The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connected to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance, routing resources. These resources interface with the rest of the routing structures through the RX and TX modules (Figure 2-41 on page 2-71). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.

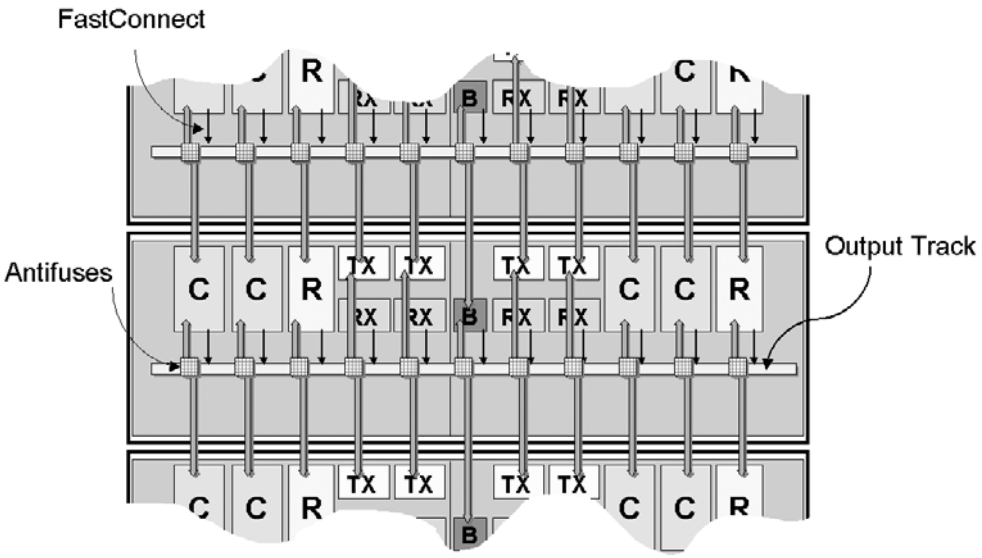


Figure 2-40 • **FastConnect Routing**

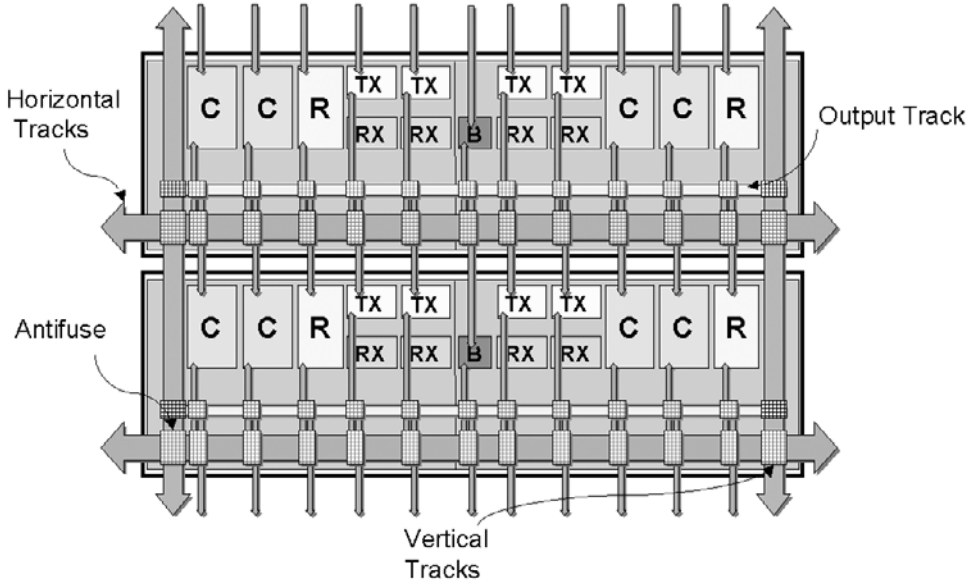


Figure 2-41 • **Horizontal and Vertical Tracks**

Timing Characteristics

Table 2-64 • **RTAX250S/SL (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Unit
		Min.	Max.	Min.	Max.	
Predicted Routing Delays						
t_{DC}	Direct connect		0.08		0.07	ns
t_{FC}	Fast connect F01		0.24		0.29	ns
t_{RD1}	Fanout 1		0.66		0.77	ns
t_{RD2}	Fanout 2		0.84		0.99	ns
t_{RD3}	Fanout 3		1.07		1.25	ns
t_{RD4}	Fanout 4		1.38		1.62	ns
t_{RD5}	Fanout 5		1.45		1.7	ns
t_{RD6}	Fanout 6		2.08		2.44	ns
t_{RD7}	Fanout 7		2.26		2.66	ns
t_{RD8}	Fanout 8		2.44		2.87	ns
t_{RD9}	Fanout 9		2.87		3.37	ns
t_{RD10}	Fanout 10		3.3		3.88	ns

Table 2-65 • **RTAX1000S/SL (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Unit
		Min.	Max.	Min.	Max.	
Predicted Routing Delays						
t_{DC}	Direct connect		0.08		0.07	ns
t_{FC}	Fast connect F01		0.24		0.29	ns
t_{RD1}	Fanout 1		0.66		0.77	ns
t_{RD2}	Fanout 2		0.84		0.99	ns
t_{RD3}	Fanout 3		1.07		1.25	ns
t_{RD4}	Fanout 4		1.38		1.62	ns
t_{RD5}	Fanout 5		1.45		1.7	ns
t_{RD6}	Fanout 6		2.08		2.44	ns
t_{RD7}	Fanout 7		2.26		2.66	ns
t_{RD8}	Fanout 8		2.44		2.87	ns
t_{RD9}	Fanout 9		2.87		3.37	ns
t_{RD10}	Fanout 10		3.3		3.88	ns

Table 2-66 • **RTAX2000S/SL (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Unit
		Min.	Max.	Min.	Max.	
Predicted Routing Delays						
t_{DC}	Direct connect		0.08		0.07	ns
t_{FC}	Fast connect F01		0.24		0.29	ns
t_{RD1}	Fanout 1		0.66		0.77	ns
t_{RD2}	Fanout 2		0.84		0.99	ns
t_{RD3}	Fanout 3		1.07		1.25	ns
t_{RD4}	Fanout 4		1.38		1.62	ns
t_{RD5}	Fanout 5		1.45		1.70	ns
t_{RD6}	Fanout 6		2.08		2.44	ns
t_{RD7}	Fanout 7		2.26		2.66	ns
t_{RD8}	Fanout 8		2.44		2.87	ns
t_{RD9}	Fanout 9		2.87		3.37	ns
t_{RD10}	Fanout 10		3.30		3.88	ns

Table 2-67 • **RTAX4000S (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'Std.' Speed		Unit
		Min.	Max.	
Predicted Routing Delays				
t_{DC}	Direct connect		0.07	ns
t_{FC}	Fast connect F01		0.29	ns
t_{RD1}	Fanout 1		0.77	ns
t_{RD2}	Fanout 2		0.99	ns
t_{RD3}	Fanout 3		1.25	ns
t_{RD4}	Fanout 4		1.62	ns
t_{RD5}	Fanout 5		1.7	ns
t_{RD6}	Fanout 6		2.44	ns
t_{RD7}	Fanout 7		2.66	ns
t_{RD8}	Fanout 8		2.87	ns
t_{RD9}	Fanout 9		3.37	ns
t_{RD10}	Fanout 10		3.88	ns

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The RTAX-S/SL family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures. In addition, these global resources have been hardened to improve SEU performance.

The RTAX-S/SL architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every RTAX-S/SL device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

Table 2-68 • **RTAX250S/SL (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HCKL}	Input Low to High		2.76		3.24	ns
t_{HCKH}	Input High to Low		2.94		3.46	ns

Table 2-69 • **RTAX250S/SL Worst-Case MPW (V_{CCA} = 1.575 V, V_{CCI} = 3.6 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HPWH}	Minimum Pulse width High	0.77		0.77		ns
t_{HPWL}	Minimum Pulse width Low	0.26		0.26		ns
f_{HMAX} [1]	Maximum frequency		649		649	MHz

Note: *$*f_{HMAX}$ = 1000/(2*(MAX(t_{HPWH}, t_{HPWL})))*

Table 2-70 • **RTAX1000S/SL (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HCKL}	Input Low to High		3.65		4.29	ns
t_{HCKH}	Input High to Low		3.48		4.09	ns

Table 2-71 • **RTAX1000S/SL Worst-Case MPW (V_{CCA} = 1.575 V, V_{CCI} = 3.6 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HPWH}	Minimum Pulse width High	0.86		0.86		ns
t_{HPWL}	Minimum Pulse width Low	0.31		0.31		ns
f_{HMAX} [1]	Maximum frequency		581		581	MHz

Note: *$*f_{HMAX}$ = 1000/(2*(MAX(t_{HPWH}, t_{HPWL})))*

Table 2-72 • **RTAX2000S/SL (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HCKL}	Input Low to High		3.65		4.29	ns
t_{HCKH}	Input High to Low		3.48		4.09	ns

Table 2-73 • **RTAX2000S/SL Worst-Case MPW (V_{CCA} = 1.575 V, V_{CCI} = 3.6 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HPWH}	Minimum Pulse width High	0.77		0.77		ns
t_{HPWL}	Minimum Pulse width Low	0.26		0.26		ns
f_{HMAX}[1]	Maximum frequency		649		649	MHz

Note: *$*f_{HMAX} = 1000/(2*(MAX(t_{HPWH}, t_{HPWL})))$*

Table 2-74 • **RTAX4000S (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'Std.' Speed		Units
		Min.	Max.	
t_{HCKL}	Input Low to High		4.37	ns
t_{HCKH}	Input High to Low		4.16	ns

Table 2-75 • **RTAX4000S Worst-Case MPW (V_{CCA} = 1.575 V, V_{CCI} = 3.6 V, T_J = 125°C)**

Parameter	Description	'Std.' Speed		Units
		Min.	Max.	
t_{HPWH}	Minimum Pulse width High	TBD		ns
t_{HPWL}	Minimum Pulse width Low	TBD		ns
f_{HMAX}[1]	Maximum frequency		TBD	MHz

Note: *$*f_{HMAX} = 1000/(2*(MAX(t_{HPWH}, t_{HPWL})))$*

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

Table 2-76 • **RTAX250S/SL (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RCKL}	Input Low to High		2.78		3.26	ns
t_{RCKH}	Input High to Low		2.92		3.43	ns
t_{RCKSW}	Maximum skew – 16 Loads		1.40		1.65	ns
	Maximum skew – 24 Loads		1.81		2.13	ns

Table 2-77 • **RTAX250S/SL Worst-Case MPW (V_{CCA} = 1.575 V, V_{CCI} = 3.6 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RPWH}	Minimum Pulse width High	0.79		0.79		ns
t_{RPWL}	Minimum Pulse width Low	0.27		0.27		ns
f_{RMAX}[1]	Maximum frequency		633		633	MHz

Note: *$*f_{RMAX} = 1000/(2*(MAX(t_{RPWH}, t_{RPWL})))$*

Table 2-78 • **RTAX1000S/SL (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RCKL}	Input Low to High		3.71		4.37	ns
t_{RCKH}	Input High to Low		3.54		4.16	ns
t_{RCKSW}	Maximum skew – 16 Loads		1.39		1.64	ns
	Maximum skew – 24 Loads		1.80		2.12	ns
	Maximum skew – 36 Loads		1.87		2.20	ns

Table 2-79 • **RTAX1000S/SL Worst-Case MPW (V_{CCA} = 1.575 V, V_{CCI} = 3.6 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RPWH}	Minimum Pulse width High	1.04		1.04		ns
t_{RPWL}	Minimum Pulse width Low	0.33		0.33		ns
f_{RMAX}[1]	Maximum frequency		481		481	MHz

Note: *$*f_{RMAX} = 1000/(2*(MAX(t_{RPWH}, t_{RPWL})))$*

Table 2-80 • **RTAX2000S/SL (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RCKL}	Input Low to High		3.71		4.37	ns
t_{RCKH}	Input High to Low		3.54		4.16	ns
t_{RCKSW}	Maximum skew – 16 Loads		1.39		1.64	ns
	Maximum skew – 24 Loads		1.80		2.12	ns
	Maximum skew – 36 Loads		2.12		2.49	ns

Table 2-81 • **RTAX2000S/SL Worst-Case MPW (V_{CCA} = 1.575 V, V_{CCI} = 3.6 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RPWH}	Minimum Pulse width High	0.79				ns
t_{RPWL}	Minimum Pulse width Low	0.27				ns
f_{RMAX}[1]	Maximum frequency		633			MHz

Note: *$*f_{RMAX} = 1000/(2*(MAX(t_{RPWH}, t_{RPWL})))$*

Table 2-82 • **RTAX4000S (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'Std.' Speed		Units
		Min.	Max.	
t_{RCKL}	Input Low to High		6.41	ns
t_{RCKH}	Input High to Low		6.19	ns
t_{RCKSW}	Maximum skew – 16 Loads		1.65	ns
	Maximum skew – 24 Loads		2.11	ns
	Maximum skew – 36 Loads		2.16	ns

Table 2-83 • **RTAX4000S Worst-Case MPW (V_{CCA} = 1.575 V, V_{CCI} = 3.6 V, T_J = 125°C)**

Parameter	Description	'Std.' Speed		Units
		Min.	Max.	
t_{RPWH}	Minimum Pulse width High	TBD		ns
t_{RPWL}	Minimum Pulse width Low	TBD		ns
f_{RMAX}[1]	Maximum frequency		TBD	MHz

Note: *$*f_{RMAX} = 1000/(2*(MAX(t_{RPWH}, t_{RPWL})))$*

Global Resource Distribution

At the root of each global resource is a ClockDistBuffer (CDB). There are two groups of four CDBs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (Figure 2-42).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 2-43).

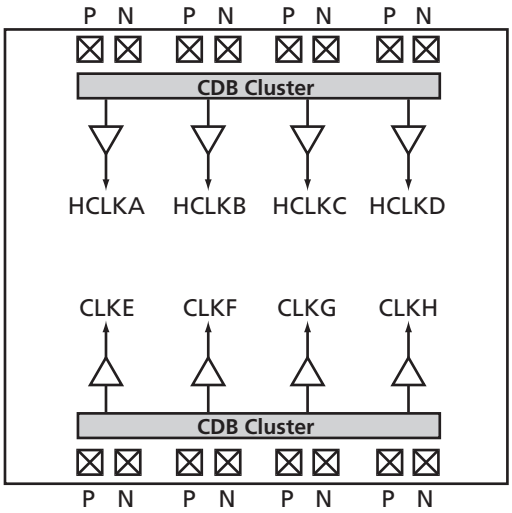


Figure 2-42 • **ClockDistBuffer Group**

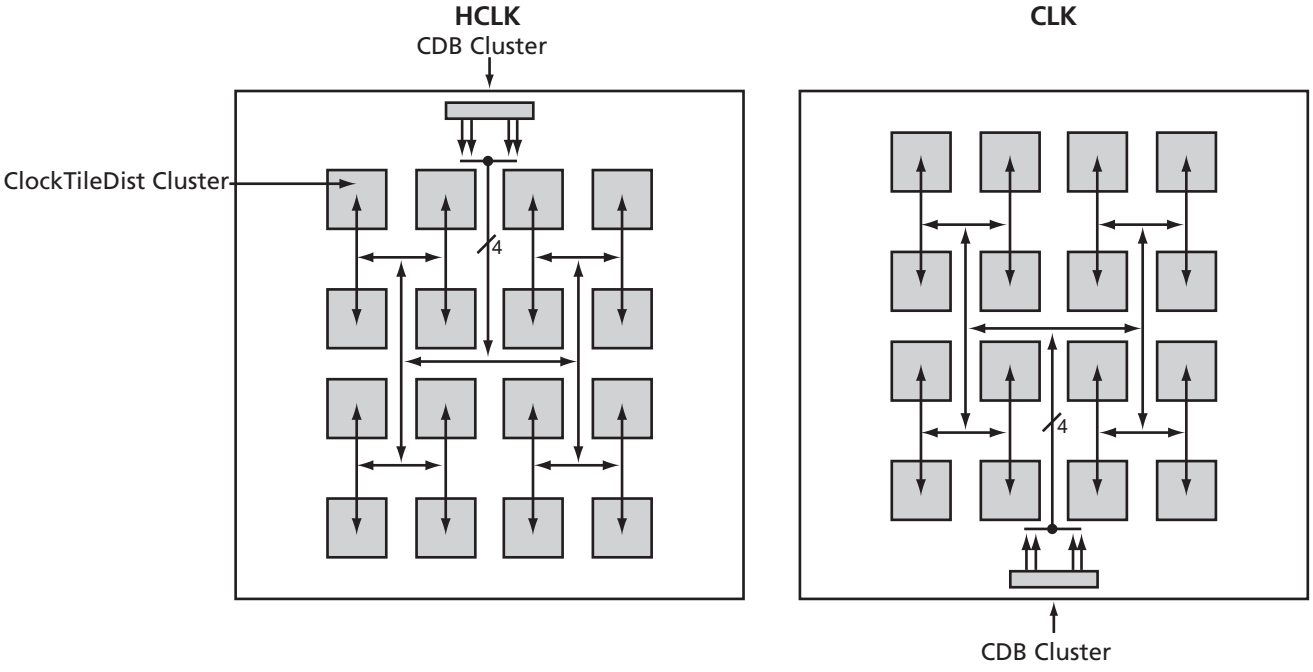


Figure 2-43 • **Example of HCLK and CLK Distributions on the RTAX2000S/SL**

The ClockTileDist Cluster contains an HCLKMux (HM) module for each of the four HCLK trees and a CLKMux (CM) module for each of the CLK trees. The HCLK branches then propagate horizontally through the middle of the core tile to HCLKColDist (HD) modules in every SuperCluster column. The CLK branches propagate vertically through the center of the core tile to CLKRowDist (RD) modules in every SuperCluster row. Together, the HCLK and CLK branches provide for a low-skew global fanout within the core tile (Figure 2-44 and Figure 2-45).

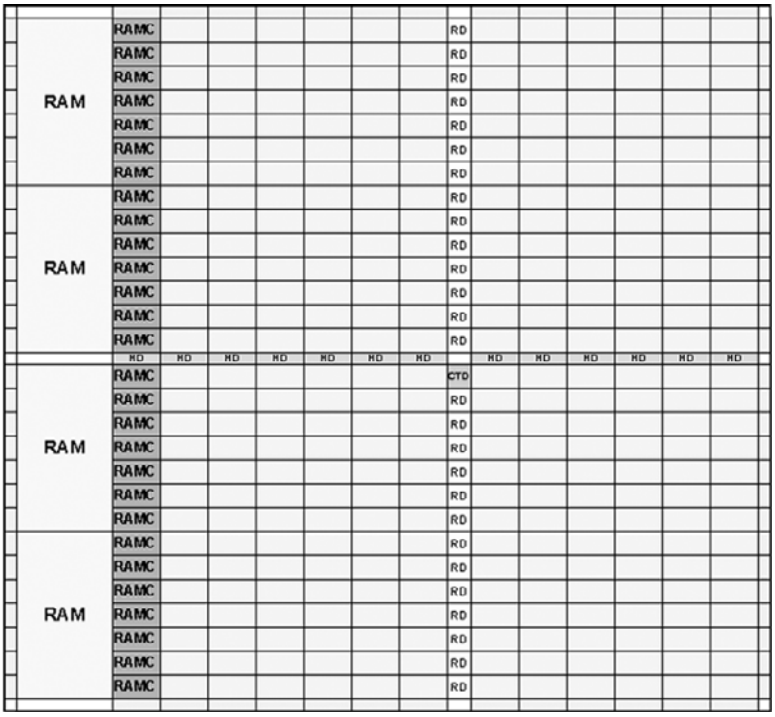


Figure 2-44 • **CTD, CD, and HD Module Layout**

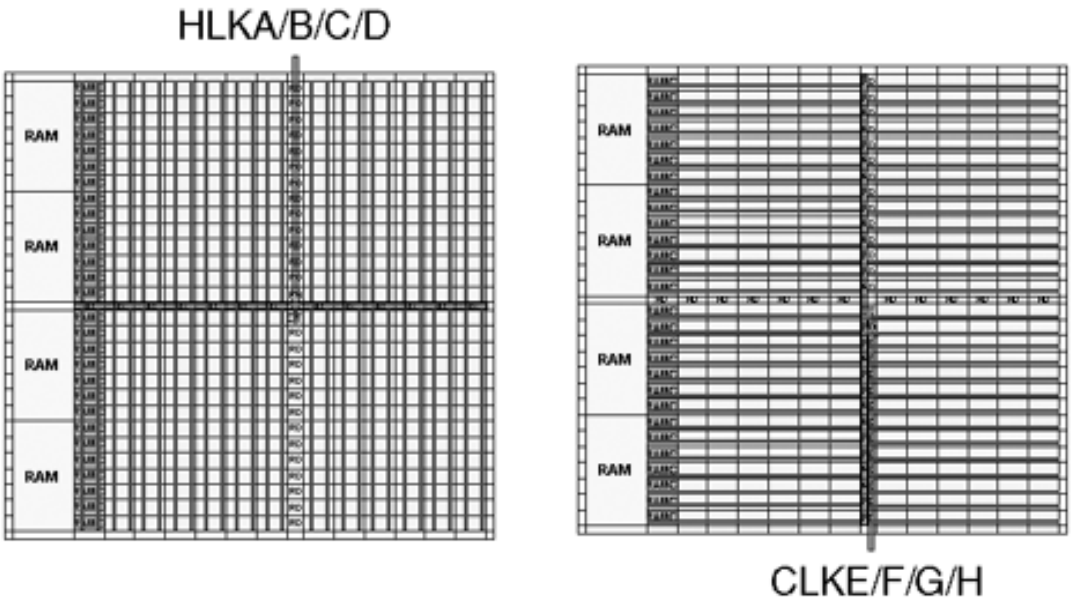


Figure 2-45 • **HCLK and CLK Distribution within a Core Tile**

The HM and CM modules can select between:

- The HCLK or CLK source
- A local signal routed on generic routing resources

This allows each core tile to have eight clocks independent of the other core tiles in the device.

Both HCLK and CLK are segmentable, meaning that individual branches of the global resource can be used independently.

Like the HM and CM modules, the HD and RD modules can select between:

- The HCLK or CLK source from the HM or CM module, respectively
- A local signal routed on generic routing resources

Again, an unused input can be tied to ground for power savings.

The RTAX-S/SL architecture is capable of supporting a large number of local clocks – 24 segments per HCLK driving north-south and 28 segments per CLK driving east-west per core tile.

Actel Designer software's place-and-route takes advantage of the segmented clock structure found in RTAX-S/SL devices by turning off any unused clock segments. This results in not only better performance but also lower power consumption. Future releases of Designer will give the user greater control over these individual clock segments.

Global Resource Access Macros

Global resources can be driven by one of three sources: external pad(s) or an internal net. These connections can be made by using one of two types of macros: CLKBUF and CLKINT.

CLKBUF and HCLKBUF

CLKBUF (HCLKBUF) is used to drive a CLK (HCLK) from external pads. These macros can be used either generically or with the specific I/O standard desired (e.g. CLKBUF_LVCMOS25, HCLKBUF_LVDS, etc.) (Figure 2-46).

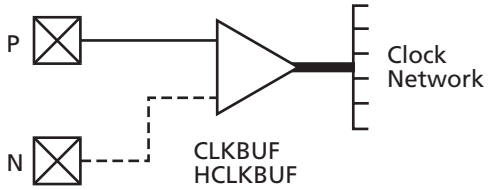


Figure 2-46 • **CLKBUF and HCLKBUF**

Package pins CLKEP and CLKEN are associated with CLKE; package pins HCLKAP and HCLKAN are associated with HCLKA, etc.

Note that when CLKBUF (HCLKBUF) is used with a single-ended I/O standard, it must be tied to the P-pad of the CLK (HCLK) package pin. In this case, the CLK (HCLK) N-pad can be used for user signals.

CLKINT and HCLKINT

CLKINT (HCLKINT) is used to access the CLK (HCLK) resource internally from the user signals (Figure 2-47).

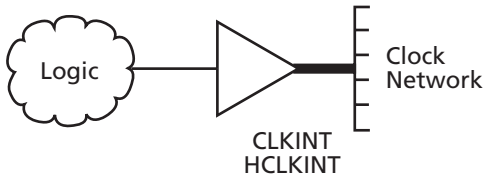


Figure 2-47 • **CLKINT and HCLKINT**

Embedded Memory

The RTAX-S/SL architecture provides extensive, high-speed memory resources to the user. Each 4,608-bit block of RAM contains its own embedded FIFO controller, allowing the user to configure each block as either RAM or FIFO.

To meet the needs of high performance designs, the memory blocks operate in synchronous mode for both read and write operations. However, the read and write clocks are completely independent, and each may operate beyond 500 MHz.

No additional core logic resources are required to cascade the address and data buses when cascading different RAM blocks. Dedicated routing runs along each column of RAM to facilitate cascading.

The RTAX-S/SL memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Since read and write operations can occur asynchronously to one another, special control circuitry is included to prevent metastability, overflow, and underflow. A block diagram of the memory module is illustrated in Figure 2-48.

During RAM operation, read (RA) and write (WA) addresses are sourced by user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Enables with programmable polarity are provided to create upper address bits for cascading up to 16 memory blocks. When cascading memory blocks, the bussed signals WA, WD, WEN, RA, RD, and REN are internally linked to eliminate external routing congestion.

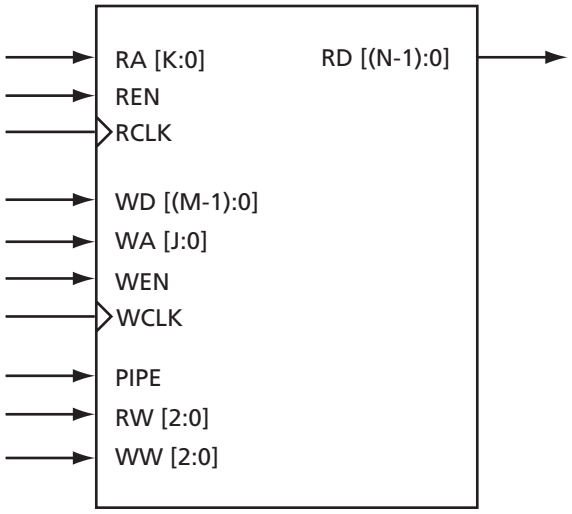


Figure 2-48 • **RTAX-S/SL Memory Module**

RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (Table 2-84). Each block has independent read and write ports, which enable simultaneous read and write operations. Simultaneous read and write operations to the same address is not supported.

Table 2-84 • **Memory Block WxD Options**

Data-Word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

RAM Configurations

The RTAX-S/SL architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The available DxW configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2, and 4kx1. The allowable RW and WW values are shown in Table 2-86.

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

Note that the RAM blocks employ little-endian byte order for read and write operations.

Table 2-85 • **RAM Signal Description**

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus.The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipeline option to be on or off.

Table 2-86 • **Allowable RW and WW Values**

RW(2:0)	WW(2:0)	D x W
000	000	4kx1
001	001	2kx2
010	010	1kx4
011	011	512x9
100	100	256x18
101	101	128x36
11x	11x	reserved

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge):

  In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting PIPE to OFF enables this mode.

- Read Pipelined (synchronous – two clock edges):

  The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.

- Write (synchronous – one clock edge):

  On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in "Timing Characteristics" on page 2-85.

Enhancing SEU Performance

SRAM structures are inherently susceptible to upsets caused by high-energy particles encountered in space. High-energy particles can cause an SRAM cell to change state, resulting in the loss or corruption of a valuable data bit. To allow users to achieve high levels of SEU performance, Actel has developed an intellectual property (IP) core to enhance the SEU tolerance of the embedded SRAM within RTAX-S/SL.

This IP employs two upset-mitigation techniques:

- Error Detection and Correction (EDAC)
- A background memory-refresher, or scrubber

The EDAC IP employs the use of shortened Hamming Codes to provide the user with single-error correction/double-error detection (SEC/DED) capabilities. These shortened Hamming Codes provide the user with an implementation that has a reduced number of logic levels and less complexity than traditional Hamming Codes. The SmartGen-generated EDAC IP supports RAM widths of 8, 16, and 32 bits, with a variable RAM depth from 256 to 4k words.

The memory scrubber circuitry has also been embedded in the EDAC IP as an optional block. The scrubber circuitry periodically refreshes memory in the background to ensure that no corruption of its contents has taken place while the memory was not in use. The refresh rate can be set by the user.

The use of EDAC IP combined with the embedded memory scrubber circuitry, gives the RTAX-S/SL an SEU radiation performance level of better than 10^{-10} errors/bit-day. See the application note *Using EDAC RAM for RadTolerant RTAX-S/SL FPGAs and Axcelerator FPGAs*.

Timing Model and Waveforms

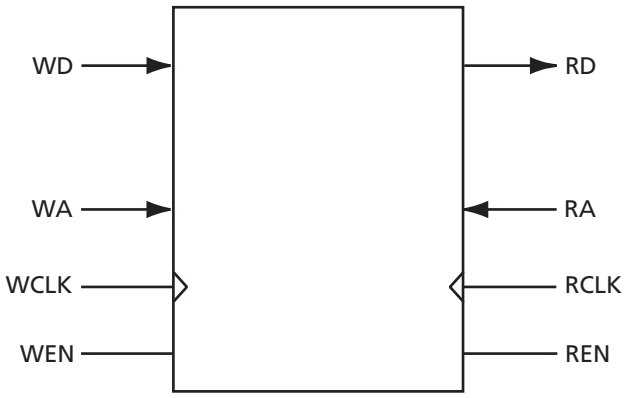


Table 2-87 • **SRAM Model**

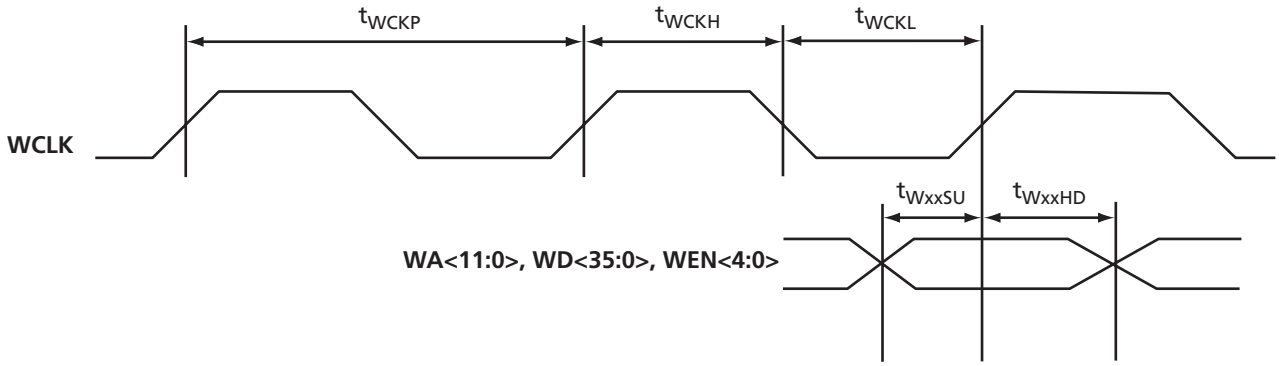


Figure 2-49 • **RAM Write Timing Waveforms**

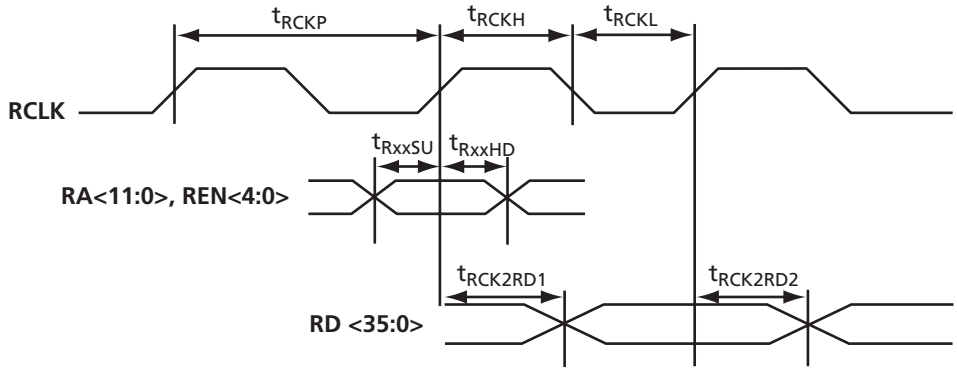


Figure 2-50 • **RAM Read Timing Waveforms**

Timing Characteristics

Table 2-88 • **One RAM Block (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	–1 Speed		Std. Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	1.45		1.70		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.30		0.35		ns
t_{WADSU}	Write Address Setup vs. WCLK	1.45		1.70		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.00		0.00		ns
t_{WENSU}	Write Enable Setup vs. WCLK	1.45		1.70		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.30		0.35		ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	0.88		0.88		ns
t_{WCKP}	WCLK Minimum Period	1.63		1.63		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	1.08		1.27		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	1.08		1.27		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		1.77		2.08	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		2.90		3.41	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.77		0.77		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	0.93		0.93		ns
t_{RCKP}	RCLK Minimum Period	1.70		1.70		ns

Note: Timing data for this single block RAM has a depth of 4,096. For all other combinations, use Actel's SmartTime tool.

Table 2-89 • **Two RAM Blocks Are Cascaded (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	1.86		2.19		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.00		0.00		ns
t_{WADSU}	Write Address Setup vs. WCLK	1.86		2.19		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.00		0.00		ns
t_{WENSU}	Write Enable Setup vs. WCLK	1.86		2.19		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.00		0.00		ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	1.76		1.76		ns
t_{WCKP}	WCLK Minimum Period	2.51		2.51		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	2.28		2.68		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	2.28		2.68		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		1.92		2.26	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.03		3.56	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	1.89		1.89		ns
t_{RCKP}	RCLK Minimum Period	2.62		2.62		ns

Note: Timing data for two cascaded RAM blocks uses a depth of 8,192. For all other combinations, use Actel's SmartTime tool.

Table 2-90 • **Four RAM Blocks Are Cascaded (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	3.17		3.73		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.00		0.00		ns
t_{WADSU}	Write Address Setup vs. WCLK	3.17		3.73		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.00		0.00		ns
t_{WENSU}	Write Enable Setup vs. WCLK	3.17		3.73		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.00		0.00		ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	2.51		2.51		ns
t_{WCKP}	WCLK Minimum Period	3.26		3.26		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	4.13		4.85		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	4.13		4.85		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		3.16		3.72	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.79		4.46	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	2.96		2.96		ns
t_{RCKP}	RCLK Minimum Period	3.69		3.69		ns

Note: Timing data for four cascaded RAM blocks uses a depth of 16,384. For all other combinations, use Actel's SmartTime tool.

Table 2-91 • **Eight RAM Blocks Are Cascaded (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	7.74		9.09		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.00		0.00		ns
t_{WADSU}	Write Address Setup vs. WCLK	7.74		9.09		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.00		0.00		ns
t_{WENSU}	Write Enable Setup vs. WCLK	7.74		9.09		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.00		0.00		ns
t_{WCKH}	WCLK Minimum High Pulse Width	0.75		0.75		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	5.13		5.13		ns
t_{WCKP}	WCLK Minimum Period	5.88		5.88		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	9.04		10.63		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	9.04		10.63		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		4.54		5.33	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		6.60		7.76	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	0.73		0.73		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	5.77		5.77		ns
t_{RCKP}	RCLK Minimum Period	6.50		6.50		ns

Note: Timing data for eight cascaded RAM blocks uses a depth of 32,768. For all other combinations, use Actel's SmartTime tool.

Table 2-92 • **Sixteen RAM Blocks Are Cascaded (Worst-Case Military Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	22.14		26.03		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.30		0.35		ns
t_{WADSU}	Write Address Setup vs. WCLK	22.14		26.03		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.30		0.35		ns
t_{WENSU}	Write Enable Setup vs. WCLK	22.14		26.03		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.30		0.35		ns
t_{WCKH}	WCLK Minimum High Pulse Width	1.31		1.54		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	23.34		27.44		ns
t_{WCKP}	WCLK Minimum Period	46.69		54.88		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	24.27		28.53		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	24.27		28.53		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		17.02		20.01	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		18.62		21.89	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	1.27		1.49		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	25.10		29.51		ns
t_{RCKP}	RCLK Minimum Period	50.21		59.02		ns

Note: Timing data for sixteen cascaded RAM blocks uses a depth of 65,536. For all other combinations, use Actel's SmartTime tool.

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various size from 4kx1 to 128x36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable Almost-Empty (AEMPTY) and Almost-Full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-51):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Note: Actel recommends that the WCLK and the RCLK are in phase with each other. For more information refer to the application note, *EMPTY and FULL Flag Behaviors of the Axcelerator FIFO Controller*.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state

The FIFO control unit was not implemented with SEU-hardened registers. Designs requiring high SEU tolerance should implement the FIFO control unit from hardened core logic.

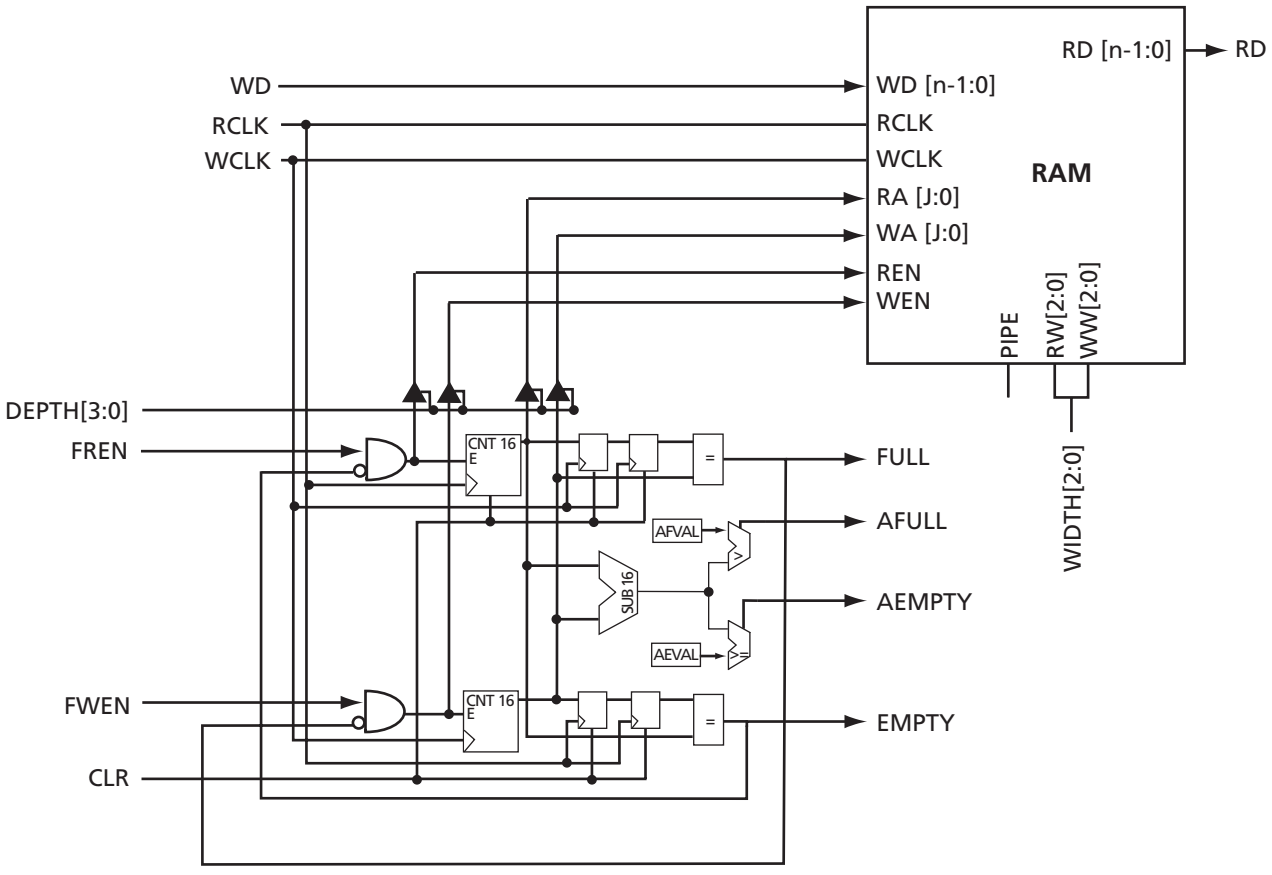


Figure 2-51 • **RTAX-S/SL RAM with Embedded FIFO Controller**

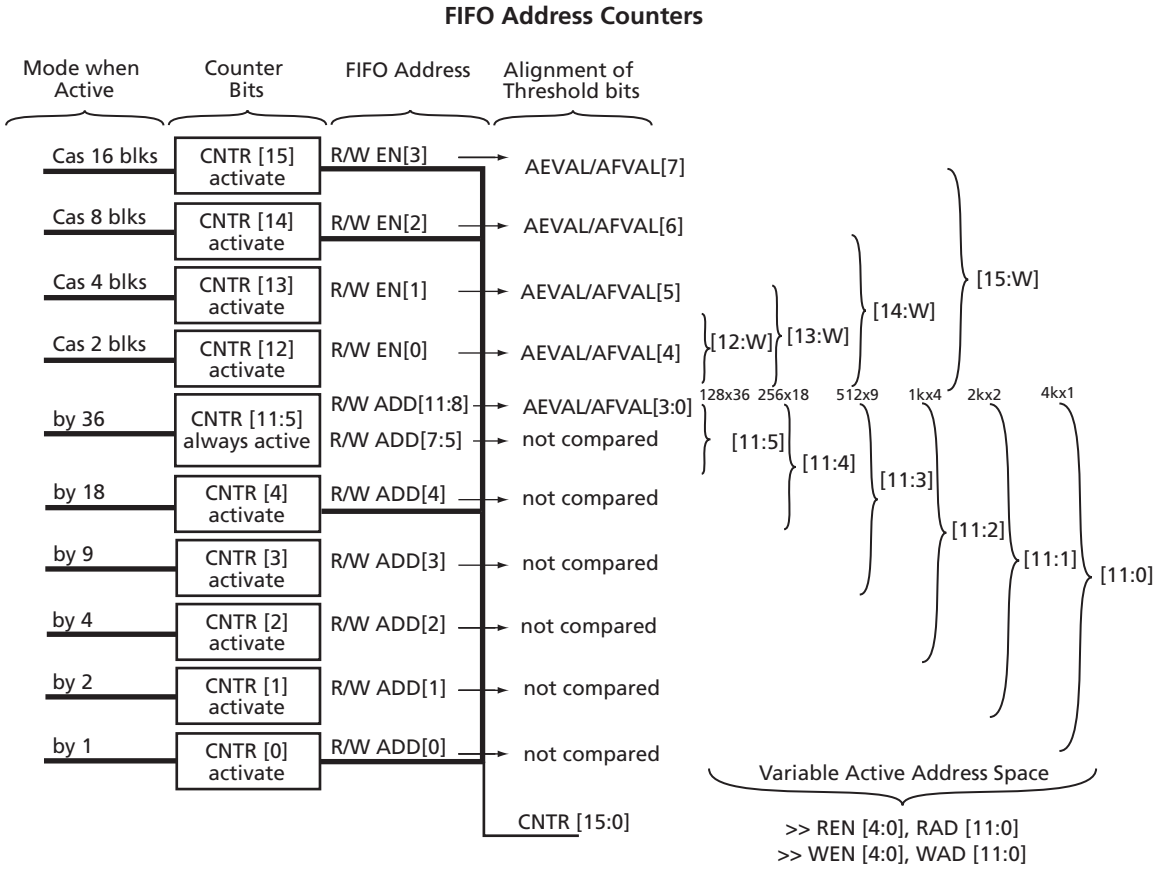
FIFO Flag Logic

The FIFO is user configurable into various depths and widths. Figure 2-52 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. Note that the effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-93).



Note: *Inactive counter bits are set to zero.*

Figure 2-52 • **FIFO Address Counters**

Table 2-93 • **FIFO Flag Logic**

Mode	Inactive AEVAL/AFVAL bits	Inactive DIFF bits (set to 0)	DIFF comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] withAE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] withAE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] withAE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] withAE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] withAE/FVAL[7:0]

Figure 2-53 illustrates flag generation. The Verilog statements for flag assignment are:

```
assign AF = (DIFF[15:0] >={AFVAL[7:0],8'b00000000})?1:0;
assign AE = ({AEVAL[7:0],8'b00000000}>=DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 2-94). The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in "Timing Characteristics" on page 2-95. For more information refer to the application note, *EMPTY and FULL Flag Behaviors of the Axcelerator FIFO Controller*.

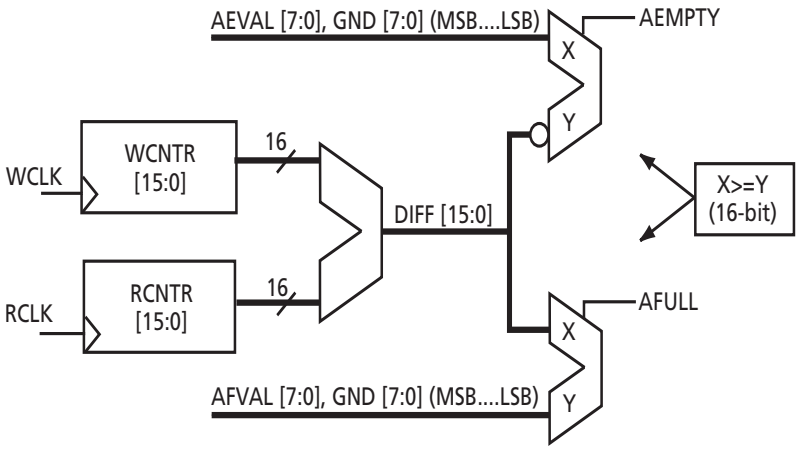


Figure 2-53 • **ALMOST-EMPTY and ALMOST-FULL Logic**

Table 2-94 • **Number of Available Configuration Bits**

Number of Blocks	Block DxW	Number of AEVAL/AFVAL Bits
1	1x1	4
2	1x2	4
2	2x1	5
4	1x4	4
4	2x2	5
4	4x1	6
8	1x8	4
8	2x4	5
8	4x2	6
8	8x1	7
16	1x16	4
16	2x8	5
16	4x4	6
16	8x2	7
16	16x1	8

Glitch Elimination

An analog filter is added to each FIFO controller to guarantee, glitch-free FIFO-flag logic.

Overflow and Underflow Control

The counter MSB keeps track of the difference between the read address (RA) and the write address (WA). The EMPTY flag is set when the read and write addresses are equal. To prevent underflow, the write address is double-sampled by the read clock prior to comparison with the read address (part A in Figure 2-54). To prevent overflow, the read address is double-sampled by the write clock prior to comparison to the write address (part B in Figure 2-54).

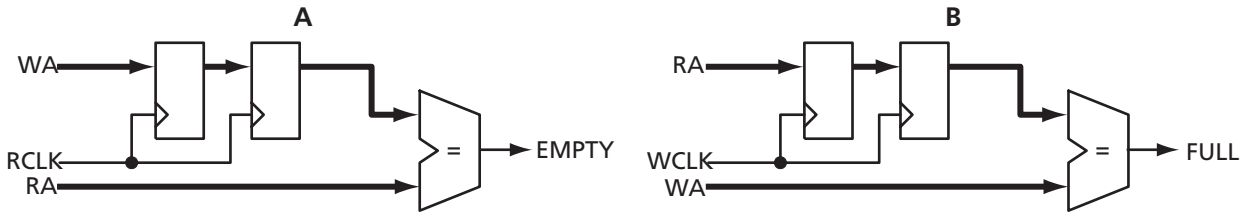


Figure 2-54 • **Overflow and Underflow Control**

FIFO Configurations

Unlike the RAM, the FIFO's write width and read width cannot be specified independently. For the FIFO, the write and read widths must be the same. The WIDTH pins are used to specify one of six allowable word widths, as shown in Table 2-95.

The DEPTH pins allow RAM cells to be cascaded to create larger FIFOs. The four pins allow depths of 2, 4, 8, and 16 to be specified. Table 2-84 on page 2-81 describes the FIFO depth options for various data width and memory blocks.

Interface

Figure 2-55 shows a logic block diagram of the RTAX-S/SL FIFO module.

Cascading FIFO Blocks

FIFO blocks can be cascaded to create deeper FIFO functions. When building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. For example, 256x36 can be configured as two blocks of 256x18. This should be taken into account when building the FIFO blocks manually. However, when using SmartGen, the user only needs to specify the depth and width of the necessary FIFO blocks. SmartGen automatically configures these blocks to optimize performance.

Clock

As with RAM configuration, the RCLK and WCLK pins have independent polarity selection

Table 2-95 • **FIFO Width Configurations**

WIDTH(2:0)	WxD
000	1x4k
001	2x2k
010	4x1k
011	9x512
100	18x256
101	36x128
11x	reserved

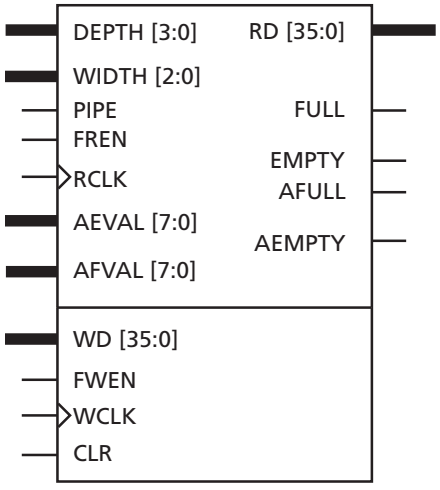


Figure 2-55 • **FIFO Block Diagram**

Table 2-96 • **FIFO Signal Description**

Signal	Direction	Description
WCLK	Input	Write clock (active either edge).
FWEN	Input	FIFO write enable. When this signal is asserted, the WD bus data is latched into the FIFO, and the internal write counters are incremented.
WD[N-1:0]	Input	Write data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
FULL	Output	Active high signal indicating that the FIFO is FULL. When this signal is set, additional write requests are ignored.
AFULL	Output	Active high signal indicating that the FIFO is AFULL.
AFVAL	Input	8-bit input defining the AFULL value of the FIFO.
RCLK	Input	Read clock (active either edge).
FREN	Input	FIFO read enable.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
EMPTY	Output	Empty flag indicating that the FIFO is EMPTY. When this signal is asserted, attempts to read the FIFO will be ignored.
AEMPTY	Output	Active high signal indicating that the FIFO is AEMPTY.
AEVAL	Input	8-bit input defining the almost-empty value of the FIFO.
PIPE	Input	Sets the pipe option on or off.
CLR	Input	Active high clear input.
DEPTH	Input	Determines the depth of the FIFO and the number of FIFOs to be cascaded.
WIDTH	Input	Determines the width of the dataword / width of the FIFO, and the number of the FIFOs to be cascaded.

Timing Characteristics

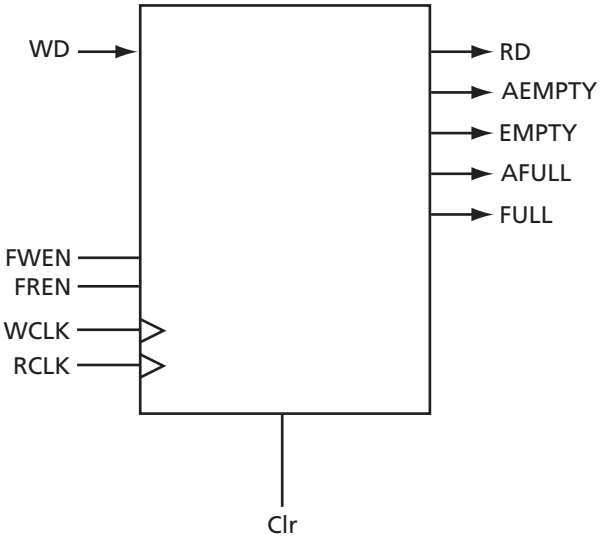


Figure 2-56 • **FIFO Model**

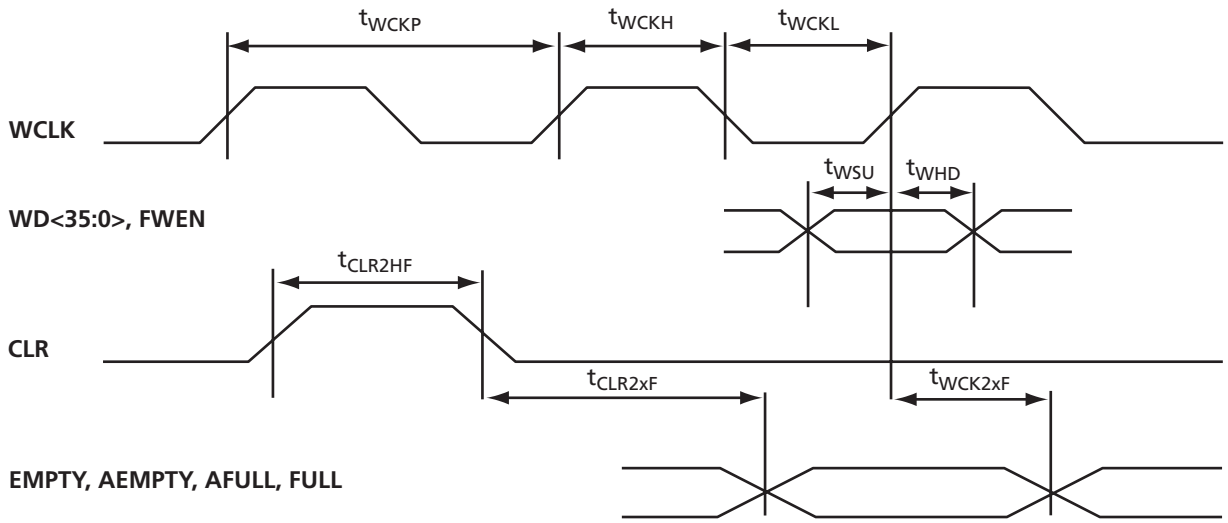


Figure 2-57 • **FIFO Write Timing**

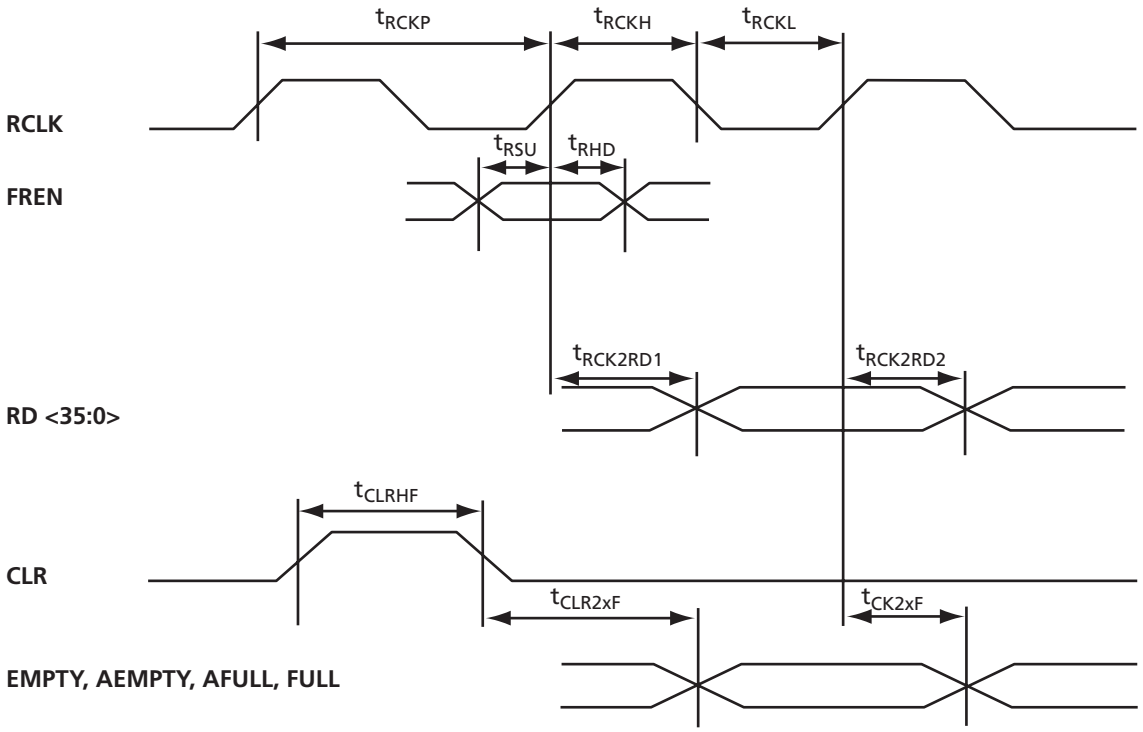


Figure 2-58 • **FIFO Read Timing**

Table 2-97 • **One FIFO Block (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	15.26		17.93		ns
t_{WHD}	Write Hold	0.30		0.35		ns
t_{WCKH}	WCLK High	0.75		0.75		ns
t_{WCKL}	WCLK Low	0.88		0.88		ns
t_{WCKP}	Minimum WCLK Period	1.63		1.63		
t_{RSU}	Read Setup	15.58		18.31		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	0.77		0.77		ns
t_{RCKL}	RCLK Low	0.93		0.93		ns
t_{RCKP}	Minimum RCLK period	1.70		1.70		
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.57		3.02		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	5.88		6.91		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.85		3.35		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	6.75		7.94		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		1.77		2.08	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.50		4.12	ns

Note: *Timing data for this single cascaded FIFO block uses a depth of 4,096. For all other combinations, please use Actel's Timing software.*

Table 2-98 • **Two FIFO Blocks Are Cascaded (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	18.40		21.64		ns
t_{WHD}	Write Hold	0.00		0.00		ns
t_{WCKH}	WCLK High	0.75		0.75		ns
t_{WCKL}	WCLK Low	1.76		1.76		ns
t_{WCKP}	Minimum WCLK Period	2.51		2.51		
t_{RSU}	Read Setup	19.18		22.55		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	0.73		0.73		ns
t_{RCKL}	RCLK Low	1.89		1.89		ns
t_{RCKP}	Minimum RCLK period	2.62		2.62		
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.57		3.02		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	5.88		6.91		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.85		3.35		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	6.75		7.94		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		1.92		2.26	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.03		3.56	ns

Note: *Timing data for two cascaded FIFO blocks uses a depth of 8,192. For all other combinations, please use Actel's Timing software.*

Table 2-99 • **Four FIFO Blocks Are Cascaded (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	19.55		22.98		ns
t_{WHD}	Write Hold	0.00		0.00		ns
t_{WCKH}	WCLK High	0.75		0.75		ns
t_{WCKL}	WCLK Low	2.51		2.51		ns
t_{WCKP}	Minimum WCLK Period	3.26		3.26		
t_{RSU}	Read Setup	20.44		24.03		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	0.73		0.73		ns
t_{RCKL}	RCLK Low	2.96		2.96		ns
t_{RCKP}	Minimum RCLK period	3.69		3.69		
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.57		3.02		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	5.88		6.91		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.85		3.35		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	6.75		7.94		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		3.16		3.72	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.79		4.46	ns

Note: *Timing data for four cascaded FIFO blocks uses a depth of 16,384. For all other combinations, please use Actel's Timing software.*

Table 2-100 • **Eight FIFO Blocks Are Cascaded (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	20.69		24.32		ns
t_{WHD}	Write Hold	0.00		0.00		ns
t_{WCKH}	WCLK High	0.75		0.75		ns
t_{WCKL}	WCLK Low	5.13		5.13		ns
t_{WCKP}	Minimum WCLK Period	5.88		5.88		
t_{RSU}	Read Setup	21.71		25.52		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	0.73		0.73		ns
t_{RCKL}	RCLK Low	5.77		5.77		ns
t_{RCKP}	Minimum RCLK period	6.50		6.50		
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.57		3.02		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	5.88		6.91		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.85		3.35		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	6.75		7.94		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		4.54		5.33	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		6.60		7.76	ns

Note: *Timing data for eight cascaded FIFO blocks uses a depth of 32,768. For all other combinations, please use Actel's Timing software.*

Table 2-101 • **Sixteen FIFO Blocks are Cascaded (Worst-Case MIlitary Conditions V_{CCA} = 1.4 V, V_{CCI} = 3.0 V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	21.85		25.69		ns
t_{WHD}	Write Hold	0.00		0.00		ns
t_{WCKH}	WCLK High	0.75		0.75		ns
t_{WCKL}	WCLK Low	13.40		13.40		ns
t_{WCKP}	Minimum WCLK Period	14.15		14.15		
t_{RSU}	Read Setup	22.97		27.00		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	0.73		0.73		ns
t_{RCKL}	RCLK Low	14.41		14.41		ns
t_{RCKP}	Minimum RCLK period	15.14		15.14		
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.57		3.02		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	5.88		6.91		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.85		3.35		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	6.75		7.94		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		16.17		19.01	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		17.18		20.19	ns

Note: *Timing data for sixteen cascaded FIFO blocks uses a depth of 65,536. For all other combinations, please use Actel's Timing software.*

Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the SmartGen core generator where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (please refer to the Actel *SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder User's Guide* for more information).
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground.

Other Architectural Features

Charge Pump Bypass

To reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The RTAX-S/SL family devices have a dedicated "V_{PUMP}" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, V_{PUMP} should be tied to GND. When the voltage level on V_{PUMP} is set to 3.3 V, the internal charge pump is turned off, and the V_{PUMP} voltage will be used as the charge pump voltage. Adequate voltage regulation (i.e., high drive, low output impedance, and good decoupling) should be used at V_{PUMP}.

JTAG

RTAX-S/SL offers a JTAG interface that is compliant with the IEEE 1149.1 standard except for the device ID length which is 33 bits. The user can employ the JTAG interface for probing a design and executing any JTAG public instructions as defined in the Table 2-102. The JTAG pins and probes are configured as a LVTTL standard port. Refer to the *IEEE Standard 1149.1 (JTAG) in the Axcelerator Family* application note, which also applies to the RTAX-S/SL family of devices. **The JTAG pins should not be left floating on flight systems.**

Table 2-102 • **JTAG Instruction Code**

Instruction (IR4:IR0)	Binary Code
EXTEST	00000
PRELOAD / SAMPLE	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
DIAGNOSTIC	10000
Reserved	All others
BYPASS	11111

Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), and an output, Test Data Out (TDO). TMS, TDI, and TRST have on-chip pull-up resistors.

TRST

TRST (Test-Logic Reset) is an active-low asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST directly to ground for flight.

There is an optional internal pull-up resistor available for the TRST input that can be set by the user at programming. Care should be exercised when using this option in combination with an external tie-off to ground.

An on-chip power-on-reset (POWRST) circuit is included. POWRST has the same function as "TRST," but it only occurs at power-up or during recovery from a V_{CCA} and/or V_{CCDA} voltage drop.

TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift_DR" state or "Shift_IR" state. The least significant bit of the selected register (i.e., IR or DR) is clocked out to TDO first by the falling edge of TCK.

TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as Boundary-Scan Register, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data bits coming out of TDO during the "Shift-IR" will be "10111." If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO_ERRORB," "PROBA_ERRORB," and "PROBB_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the "PROBA_ERRORB" is used as a "Power-up done successfully" flag.

During flight, the following configurations for all JTAG and Probe pins are recommended (Table 2-103 on page 2-101).

Table 2-103 • **JTAG and Probe Pin Recommendations for Flight**

JTAG and Probe Pins	Configurations
TCK	• Can be hardwired to V_{CCDA} or ground • Can be driven to V_{CCDA} or ground • Must not be left unterminated
TDO	Must be left unconnected
TDI	• Can be hardwired or driven to V_{CCDA} • Can be left unconnected (equipped with internal 10 k pull-up resistor)
TMS	• Can be hardwired or driven to V_{CCDA} • Can be left unconnected (equipped with internal 10 k pull-up resistor)
TRST	Must be hardwired to ground (equipped with optional internal 10 k pull-up resistor)
PRA/B/C/D	Must be left unconnected

Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

1. IDCODE:

   The IDCODE is a 33-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Actel identity, part number, and version number in a specific JTAG format. Refer to the *IEEE Standard 1149.1 (JTAG) in the Axcelerator Family* application note for more information.

2. USERCODE:

   The USERCODE is a 33-bit programmable JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed. Refer to the *IEEE Standard 1149.1 (JTAG) in the Axcelerator Family* application note for more information.

3. Boundary-Scan Register (BSR):

   Each I/O contains three BSR Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the BSR. The length of the BSR is the number of I/Os in the die (not the package) multiplied by three. This excludes special function pins (TRST, TCK, TMS, TDI, TDO, PRA, PRB, PRC, PRD, and VPUMP).

4. Bypass Register (BYR):

   This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

Special Fuses

Security

Actel antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus making device cloning impossible. In addition, special security fuses are hidden throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an RTAX-S/SL device that access or bypass these security fuses will destroy access to the rest of the device. (refer to the *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper).

Look for this symbol to ensure your valuable IP is secure.

Figure 2-59 • **FuseLock Logo**

To ensure maximum security in RTAX-S/SL devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

Global Set Fuse

The Global Set Fuse determines if all R-cells and I/O Registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers ("R-Cell" on page 2-66). Default setting is to clear all registers (GCLR = 0 and GPSET =1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET= 0). A local CLR or PRESET will take precedence overt this setting. Both pins are pulled HIGH during normal device operation. For use details, see Libero IDE online help.

Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles the integrity of the design is maintained throughout the debug process.

Each member of the RTAX-S/SL family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the RTAX-S/SL device. Each core tile can has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed (see "Special Fuses" on page 2-101 for more information).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-9 on page 1-8). Once the design has been placed-and-routed, and the RTAX-S/SL device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

Programming

Device programming is supported through the Silicon Sculptor 3, a single-site, robust and compact device programmer for the PC. Up to four Silicon Sculptor 3s can be daisy-chained and controlled from a single PC host. With standalone software for the PC, Silicon Sculptor 3 is designed to allow concurrent programming of multiple units from the same PC when daisy-chained.

Silicon Sculptor 3 programs devices independently to achieve the fastest programming times possible. Each fuse is verified by Silicon Sculptor 3 to ensure correct programming. Furthermore, at the end of programming, there are integrity tests that are run to ensure that programming was completed properly. Not only does it test programmed and nonprogrammed fuses, Silicon Sculptor 3 also provides a self-test to test its own hardware extensively.

Programming an RTAX-S/SL device using Silicon Sculptor 3 is similar to programming any other antifuse device. The procedure is as follows:

1. Load the AFM file.
2. Select the device to be programmed.
3. Begin programming.

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via our In-House Programming Center.

For more details on programming the RTAX-S/SL devices, please refer to the *Silicon Sculptor User's Guide*.

Package Pin Assignments

208-Pin CQFP

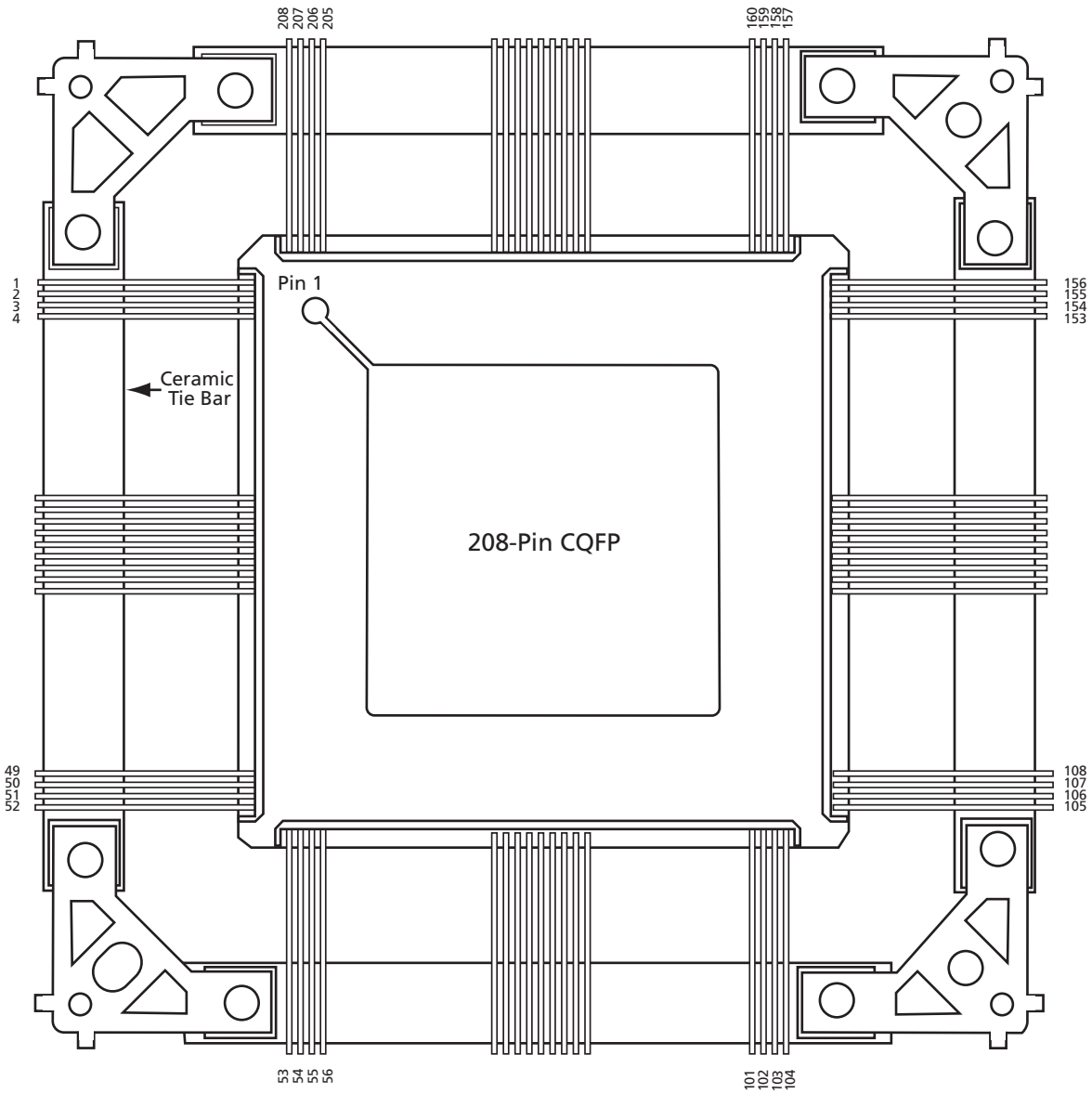


Figure 3-1 • **208-Pin CQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

208 CQFP	
RTAX250S/SL Function	**Pin Number**
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

208 CQFP	
RTAX250S/SL Function	**Pin Number**
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

208 CQFP	
RTAX250S/SL Function	**Pin Number**
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

208 CQFP	
RTAX250S/SL Function	**Pin Number**
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

208 CQFP	
RTAX250S/SL Function	**Pin Number**
GND	194
GND	196
GND	201
GND	208
NC	72
NC	73
NC	74
NC	75
NC	83
NC	84
NC	85
NC	86
NC	176
NC	177
NC	178
NC	179
NC	187
NC	188
NC	189
NC	190
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
V_{CCA}	2
V_{CCA}	14
V_{CCA}	38
V_{CCA}	52
V_{CCA}	64
V_{CCA}	93
V_{CCA}	118
V_{CCA}	142

208 CQFP	
RTAX250S/SL Function	**Pin Number**
V_{CCA}	156
V_{CCA}	168
V_{CCA}	195
V_{CCDA}	1
V_{CCDA}	26
V_{CCDA}	53
V_{CCDA}	63
V_{CCDA}	78
V_{CCDA}	95
V_{CCDA}	105
V_{CCDA}	130
V_{CCDA}	157
V_{CCDA}	167
V_{CCDA}	182
V_{CCDA}	202
$V_{CCI}B0$	193
$V_{CCI}B0$	200
$V_{CCI}B1$	163
$V_{CCI}B1$	172
$V_{CCI}B2$	135
$V_{CCI}B2$	149
$V_{CCI}B3$	112
$V_{CCI}B3$	124
$V_{CCI}B4$	89
$V_{CCI}B4$	98
$V_{CCI}B5$	58
$V_{CCI}B5$	68
$V_{CCI}B6$	31
$V_{CCI}B6$	45
$V_{CCI}B7$	8
$V_{CCI}B7$	20
V_{PUMP}	158

256-Pin CQFP

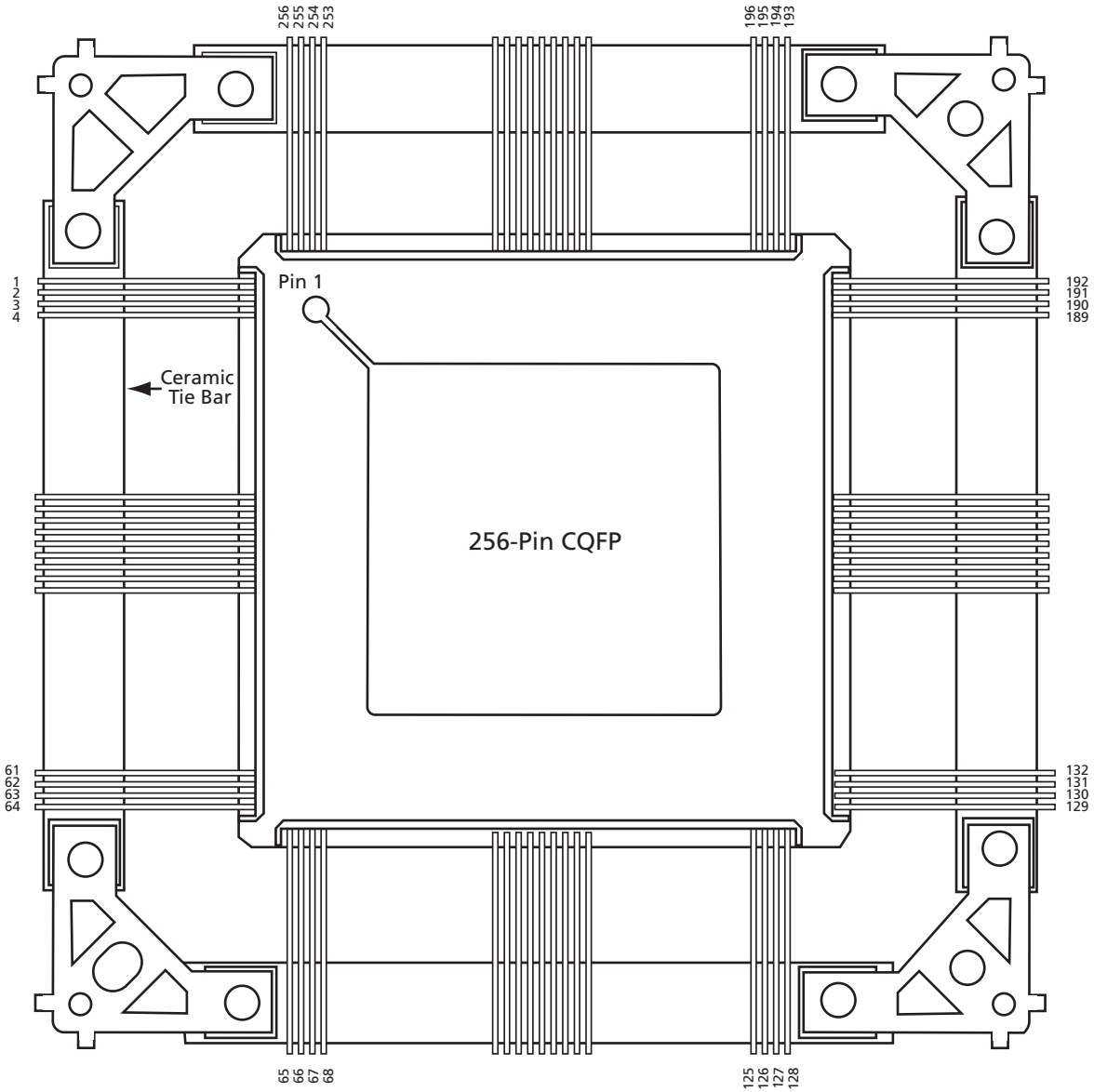


Figure 3-2 • **256-Pin CQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

256-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
Bank 0	
IO01NB0F0	248
IO01PB0F0	249
IO04NB0F0	246
IO04PB0F0	247
IO05NB0F0	242
IO05PB0F0	243
IO08NB0F0	240
IO08PB0F0	241
Bank 0	
IO37NB0F3	234
IO37PB0F3	235
IO41NB0F3/HCLKAN	232
IO41PB0F3/HCLKAP	233
IO42NB0F3/HCLKBN	228
IO42PB0F3/HCLKBP	229
Bank 1 -	
IO43NB1F4/HCLKCN	220
IO43PB1F4/HCLKCP	221
IO44NB1F4/HCLKDN	216
IO44PB1F4/HCLKDP	217
Bank 1	
IO65NB1F6	210
IO65PB1F6	211
IO69NB1F6	208
IO69PB1F6	209
IO70NB1F6	199
IO71NB1F6	204
IO71PB1F6	205
IO73NB1F6	202
IO73PB1F6	203
IO74NB1F6	197
IO74PB1F6	198
Bank 2	
IO87NB2F8	187
IO87PB2F8	188
IO89PB2F8	186

256-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
Bank 2	
IO107NB2F10	184
IO107PB2F10	185
IO110NB2F10	180
IO110PB2F10	181
IO111NB2F10	178
IO111PB2F10	179
IO112NB2F10	174
IO112PB2F10	175
IO113NB2F10	172
IO113PB2F10	173
IO114NB2F10	168
IO114PB2F10	169
IO115NB2F10	166
IO115PB2F10	167
IO117NB2F10	162
IO117PB2F10	163
Bank 3	
IO139NB3F13	158
IO139PB3F13	159
IO141NB3F13	154
IO141PB3F13	155
IO142NB3F13	152
IO142PB3F13	153
IO145NB3F13	148
IO145PB3F13	149
IO146NB3F13	146
IO146PB3F13	147
IO147NB3F13	140
IO147PB3F13	141
IO148NB3F13	142
IO148PB3F13	143
IO149NB3F13	136
IO149PB3F13	137
Bank 3	
IO165NB3F15	135
IO167NB3F15	133

256-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
IO167PB3F15	134
Bank 4	
IO181NB4F17	124
IO181PB4F17	125
IO182NB4F17	122
IO182PB4F17	123
IO183NB4F17	118
IO183PB4F17	119
IO184NB4F17	116
IO184PB4F17	117
IO190NB4F17	112
IO190PB4F17	113
IO192NB4F17	110
IO192PB4F17	111
Bank 4	
IO212NB4F19/CLKEN	104
IO212PB4F19/CLKEP	105
IO213NB4F19/CLKFN	100
IO213PB4F19/CLKFP	101
Bank 5	
IO214NB5F20/CLKGN	92
IO214PB5F20/CLKGP	93
IO215NB5F20/CLKHN	88
IO215PB5F20/CLKHP	89
Bank 5	
IO236NB5F22	82
IO236PB5F22	83
IO238NB5F22	80
IO238PB5F22	81
IO240NB5F22	76
IO240PB5F22	77
IO242NB5F22	74
IO242PB5F22	75
IO243NB5F22	70
IO243PB5F22	71
IO244NB5F22	68
IO244PB5F22	69

256-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
Bank 6	
IO257PB6F24	60
IO258NB6F24	58
IO258PB6F24	59
Bank 6	
IO279NB6F26	56
IO279PB6F26	57
IO280NB6F26	52
IO280PB6F26	53
IO281NB6F26	50
IO281PB6F26	51
IO282NB6F26	46
IO282PB6F26	47
IO284NB6F26	44
IO284PB6F26	45
IO285NB6F26	40
IO285PB6F26	41
IO286NB6F26	38
IO286PB6F26	39
IO287NB6F26	34
IO287PB6F26	35
Bank 7 9	
IO310NB7F29	30
IO310PB7F29	31
IO311NB7F29	26
IO311PB7F29	27
IO312NB7F29	24
IO312PB7F29	25
IO315NB7F29	20
IO315PB7F29	21
IO316NB7F29	18
IO316PB7F29	19
IO317NB7F29	14
IO317PB7F29	15
IO318NB7F29	12
IO318PB7F29	13
IO320NB7F29	8

256-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
IO320PB7F29	9
Bank 7	
IO341NB7F31	6
IO341PB7F31	7
Dedicated I/O	
GND	1
GND	5
GND	11
GND	17
GND	23
GND	29
GND	33
GND	37
GND	43
GND	49
GND	55
GND	62
GND	64
GND	65
GND	73
GND	79
GND	85
GND	91
GND	97
GND	103
GND	109
GND	115
GND	121
GND	128
GND	129
GND	132
GND	139
GND	145
GND	151
GND	157
GND	161
GND	165

256-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
GND	171
GND	177
GND	183
GND	190
GND	192
GND	193
GND	201
GND	207
GND	213
GND	219
GND	225
GND	231
GND	239
GND	245
GND	256
PRA	227
PRB	226
PRC	99
PRD	98
TCK	253
TDI	252
TDO	250
TMS	254
TRST	255
V_{CCA}	3
V_{CCA}	4
V_{CCA}	22
V_{CCA}	42
V_{CCA}	61
V_{CCA}	63
V_{CCA}	84
V_{CCA}	108
V_{CCA}	127
V_{CCA}	131
V_{CCA}	150
V_{CCA}	170
V_{CCA}	189

256-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
V_{CCA}	191
V_{CCA}	212
V_{CCA}	238
V_{CCDA}	2
V_{CCDA}	32
V_{CCDA}	66
V_{CCDA}	67
V_{CCDA}	86
V_{CCDA}	87
V_{CCDA}	94
V_{CCDA}	95
V_{CCDA}	96
V_{CCDA}	106
V_{CCDA}	107
V_{CCDA}	126
V_{CCDA}	130
V_{CCDA}	160
V_{CCDA}	194
V_{CCDA}	196
V_{CCDA}	214
V_{CCDA}	215
V_{CCDA}	222
V_{CCDA}	223
V_{CCDA}	224
V_{CCDA}	236
V_{CCDA}	237
V_{CCDA}	251
$V_{CCI}B0$	230
$V_{CCI}B0$	244
$V_{CCI}B1$	200
$V_{CCI}B1$	206
$V_{CCI}B1$	218
$V_{CCI}B2$	164
$V_{CCI}B2$	176
$V_{CCI}B2$	182
$V_{CCI}B3$	138
$V_{CCI}B3$	144

256-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B3$	156
$V_{CCI}B4$	102
$V_{CCI}B4$	114
$V_{CCI}B4$	120
$V_{CCI}B5$	72
$V_{CCI}B5$	78
$V_{CCI}B5$	90
$V_{CCI}B6$	36
$V_{CCI}B6$	48
$V_{CCI}B6$	54
$V_{CCI}B7$	10
$V_{CCI}B7$	16
$V_{CCI}B7$	28
V_{PUMP}	195

352-Pin CQFP

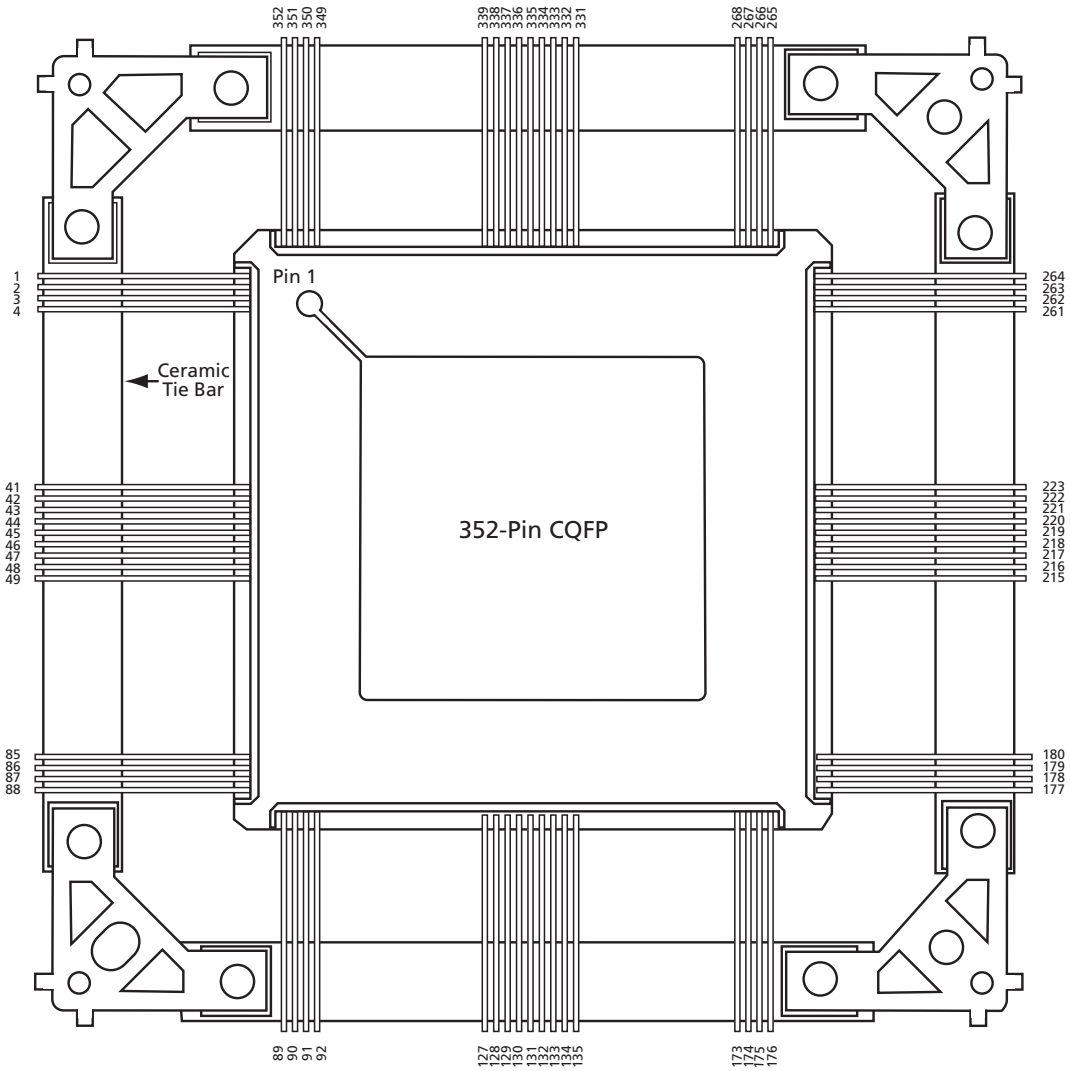


Figure 3-3 • **352-Pin CQFP**

Note:

The 352-pin CQFP pin assignments for RTAX250S/SL, RTAX1000S/SL and RTAX2000S/SL are compatible except for the following pins.

Table 3-1 • **Compatibility Table for the CQ352 Package**

	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
RTAX250S/SL	NA	117, 148, 294, 327, 328,	91, 117, 130, 131, 148, 174, 268, 294, 307, 308, 327, 328,	Not Pin Compatible
RTAX1000S/SL	117, 148, 294, 327, 328,	NA	91,130, 131, 174, 268, 307, 308	Not Pin Compatible
RTAX2000S/SL	91, 117, 130, 131, 148, 174, 268, 294, 307, 308, 327, 328,	91,130, 131, 174, 268, 307, 308	NA	Not Pin Compatible

Where exceptions occur, the smaller density devices have those pins designated as No Connects (NC). Customers are therefore recommended to layout their board targeting the larger density device, in order to preserve interchangeability between the two devices. Note: RTAX4000S is not pin compatible with any of the smaller density devices.

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
Bank 0	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313
IO13PB0F0/HCLKBP	314
Bank 1	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282
IO24NB1F1	275
IO24PB1F1	276

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
Bank 2	
IO29NB2F2	261
IO29PB2F2	262
IO30NB2F2	259
IO30PB2F2	260
IO31NB2F2	255
IO31PB2F2	256
IO33NB2F2	249
IO33PB2F2	250
IO34NB2F2	253
IO34PB2F2	254
IO35NB2F2	247
IO35PB2F2	248
IO36NB2F2	243
IO36PB2F2	244
IO37NB2F2	241
IO37PB2F2	242
IO38NB2F2	237
IO38PB2F2	238
IO39NB2F2	235
IO39PB2F2	236
IO41NB2F2	231
IO41PB2F2	232
IO42NB2F2	229
IO42PB2F2	230
IO43NB2F2	225
IO43PB2F2	226
IO44NB2F2	223
IO44PB2F2	224
Bank 3	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
Bank 4	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166
IO64PB4F4	167
IO65NB4F4	170
IO65PB4F4	171
IO66NB4F4	164
IO66PB4F4	165
IO67NB4F4	160

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
IO67PB4F4	161
IO68NB4F4	158
IO68PB4F4	159
IO70NB4F4	154
IO70PB4F4	155
IO72NB4F4	152
IO72PB4F4	153
IO73NB4F4	146
IO73PB4F4	147
IO74NB4F4/CLKEN	142
IO74PB4F4/CLKEP	143
IO75NB4F4/CLKFN	136
IO75PB4F4/CLKFP	137
Bank 5	
IO76NB5F5/CLKGN	128
IO76PB5F5/CLKGP	129
IO77NB5F5/CLKHN	122
IO77PB5F5/CLKHP	123
IO78NB5F5	112
IO78PB5F5	113
IO79NB5F5	118
IO79PB5F5	119
IO80NB5F5	110
IO80PB5F5	111
IO82NB5F5	106
IO82PB5F5	107
IO84NB5F5	100
IO84PB5F5	101
IO85NB5F5	104
IO85PB5F5	105
IO86NB5F5	98
IO86PB5F5	99
IO87NB5F5	94
IO87PB5F5	95
IO89NB5F5	92
IO89PB5F5	93
Bank 6	

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
IO90PB6F6	86
IO91NB6F6	84
IO91PB6F6	85
IO92NB6F6	78
IO92PB6F6	79
IO93NB6F6	82
IO93PB6F6	83
IO95NB6F6	76
IO95PB6F6	77
IO96NB6F6	72
IO96PB6F6	73
IO97NB6F6	70
IO97PB6F6	71
IO98NB6F6	66
IO98PB6F6	67
IO99NB6F6	64
IO99PB6F6	65
IO100NB6F6	60
IO100PB6F6	61
IO101NB6F6	58
IO101PB6F6	59
IO103NB6F6	54
IO103PB6F6	55
IO104NB6F6	52
IO104PB6F6	53
IO105NB6F6	48
IO105PB6F6	49
IO106NB6F6	46
IO106PB6F6	47
Bank 7	
IO107NB7F7	40
IO107PB7F7	41
IO108NB7F7	42
IO108PB7F7	43
IO109NB7F7	36
IO109PB7F7	37
IO110NB7F7	34

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
IO110PB7F7	35
IO111NB7F7	30
IO111PB7F7	31
IO113NB7F7	28
IO113PB7F7	29
IO114NB7F7	24
IO114PB7F7	25
IO115NB7F7	22
IO115PB7F7	23
IO116NB7F7	18
IO116PB7F7	19
IO117NB7F7	16
IO117PB7F7	17
IO118NB7F7	12
IO118PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121NB7F7	6
IO121PB7F7	7
IO123NB7F7	4
IO123PB7F7	5
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88

352-Pin CQFP	
RTAX250S/SL Function	Pin Number
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330

352-Pin CQFP	
RTAX250S/SL Function	Pin Number
GND	334
GND	340
GND	345
GND	352
NC	91
NC	117
NC	124
NC	125
NC	126
NC	127
NC	130
NC	131
NC	138
NC	139
NC	140
NC	141
NC	148
NC	174
NC	268
NC	294
NC	301
NC	302
NC	303
NC	304
NC	307
NC	308
NC	315
NC	316
NC	317
NC	318
NC	327
NC	328
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349

352-Pin CQFP	
RTAX250S/SL Function	Pin Number
TDI	348
TDO	347
TMS	350
TRST	351
V_{CCA}	3
V_{CCA}	14
V_{CCA}	32
V_{CCA}	56
V_{CCA}	74
V_{CCA}	87
V_{CCA}	102
V_{CCA}	114
V_{CCA}	150
V_{CCA}	162
V_{CCA}	175
V_{CCA}	191
V_{CCA}	209
V_{CCA}	233
V_{CCA}	251
V_{CCA}	263
V_{CCA}	279
V_{CCA}	291
V_{CCA}	329
V_{CCA}	339
V_{CCDA}	2
V_{CCDA}	44
V_{CCDA}	90
V_{CCDA}	116
V_{CCDA}	132
V_{CCDA}	149
V_{CCDA}	178
V_{CCDA}	221
V_{CCDA}	266
V_{CCDA}	293
V_{CCDA}	309
V_{CCDA}	346
$V_{CCI}B0$	321

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
$V_{CCI}B0$	333
$V_{CCI}B0$	344
$V_{CCI}B1$	273
$V_{CCI}B1$	285
$V_{CCI}B1$	297
$V_{CCI}B2$	227
$V_{CCI}B2$	239
$V_{CCI}B2$	245
$V_{CCI}B2$	257
$V_{CCI}B3$	185

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
$V_{CCI}B3$	197
$V_{CCI}B3$	203
$V_{CCI}B3$	215
$V_{CCI}B4$	144
$V_{CCI}B4$	156
$V_{CCI}B4$	168
$V_{CCI}B5$	96
$V_{CCI}B5$	108
$V_{CCI}B5$	120

352-Pin CQFP	
RTAX250S/SL Function	**Pin Number**
$V_{CCI}B6$	50
$V_{CCI}B6$	62
$V_{CCI}B6$	68
$V_{CCI}B6$	80
$V_{CCI}B7$	8
$V_{CCI}B7$	20
$V_{CCI}B7$	26
$V_{CCI}B7$	38
V_{PUMP}	267

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
Bank 0	
IO02NB0F0	341
IO02PB0F0	342
IO03PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO08NB0F0	331
IO08PB0F0	332
IO09NB0F0	335
IO09PB0F0	336
IO24NB0F2	325
IO24PB0F2	326
IO25NB0F2	323
IO25PB0F2	324
IO30NB0F2/HCLKAN	319
IO30PB0F2/HCLKAP	320
IO31NB0F2/HCLKBN	313
IO31PB0F2/HCLKBP	314
Bank 1	
IO32NB1F3/HCLKCN	305
IO32PB1F3/HCLKCP	306
IO33NB1F3/HCLKDN	299
IO33PB1F3/HCLKDP	300
IO38NB1F3	295
IO38PB1F3	296
IO54NB1F5	287
IO54PB1F5	288
IO55NB1F5	289
IO55PB1F5	290
IO56NB1F5	281
IO56PB1F5	282
IO57NB1F5	283
IO57PB1F5	284
IO59NB1F5	277
IO59PB1F5	278
IO60NB1F5	275
IO60PB1F5	276

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
IO61NB1F5	271
IO61PB1F5	272
IO63NB1F5	269
IO63PB1F5	270
Bank 2	
IO64NB2F6	259
IO64PB2F6	260
IO67NB2F6	261
IO67PB2F6	262
IO68NB2F6	255
IO68PB2F6	256
IO69NB2F6	253
IO69PB2F6	254
IO74NB2F7	249
IO74PB2F7	250
IO75NB2F7	247
IO75PB2F7	248
IO76NB2F7	243
IO76PB2F7	244
IO77NB2F7	241
IO77PB2F7	242
IO78NB2F7	237
IO78PB2F7	238
IO79NB2F7	235
IO79PB2F7	236
IO82NB2F7	231
IO82PB2F7	232
IO83NB2F7	229
IO83PB2F7	230
IO94NB2F8	225
IO94PB2F8	226
IO95NB2F8	223
IO95PB2F8	224
Bank 3	
IO96NB3F9	217
IO96PB3F9	218
IO97NB3F9	219

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
IO97PB3F9	220
IO99NB3F9	213
IO99PB3F9	214
IO108NB3F10	211
IO108PB3F10	212
IO109NB3F10	207
IO109PB3F10	208
IO111NB3F10	205
IO111PB3F10	206
IO112NB3F10	199
IO112PB3F10	200
IO113NB3F10	201
IO113PB3F10	202
IO115NB3F10	195
IO115PB3F10	196
IO116NB3F10	193
IO116PB3F10	194
IO117NB3F10	189
IO117PB3F10	190
IO124NB3F11	183
IO124PB3F11	184
IO125NB3F11	187
IO125PB3F11	188
IO127NB3F11	181
IO127PB3F11	182
IO128NB3F11	179
IO128PB3F11	180
Bank 4	
IO130NB4F12	172
IO130PB4F12	173
IO131NB4F12	170
IO131PB4F12	171
IO132NB4F12	166
IO132PB4F12	167
IO133NB4F12	164
IO133PB4F12	165
IO134NB4F12	160

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
IO134PB4F12	161
IO136NB4F12	158
IO136PB4F12	159
IO137NB4F12	154
IO137PB4F12	155
IO138NB4F12	152
IO138PB4F12	153
IO153NB4F14	146
IO153PB4F14	147
IO159NB4F14/CLKEN	142
IO159PB4F14/CLKEP	143
IO160NB4F14/CLKFN	136
IO160PB4F14/CLKFP	137
Bank 5	
IO161NB5F15/CLKGN	128
IO161PB5F15/CLKGP	129
IO162NB5F15/CLKHN	122
IO162PB5F15/CLKHP	123
IO167NB5F15	118
IO167PB5F15	119
IO183NB5F17	110
IO183PB5F17	111
IO184NB5F17	112
IO184PB5F17	113
IO185NB5F17	104
IO185PB5F17	105
IO186NB5F17	106
IO186PB5F17	107
IO187NB5F17	98
IO187PB5F17	99
IO188NB5F17	100
IO188PB5F17	101
IO190NB5F17	94
IO190PB5F17	95
IO192NB5F17	92
IO192PB5F17	93
Bank 6	

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
IO193PB6F18	86
IO194NB6F18	84
IO194PB6F18	85
IO196NB6F18	78
IO196PB6F18	79
IO197NB6F18	82
IO197PB6F18	83
IO198NB6F18	76
IO198PB6F18	77
IO203NB6F19	72
IO203PB6F19	73
IO204NB6F19	70
IO204PB6F19	71
IO205NB6F19	66
IO205PB6F19	67
IO206NB6F19	64
IO206PB6F19	65
IO207NB6F19	60
IO207PB6F19	61
IO208NB6F19	58
IO208PB6F19	59
IO211NB6F19	54
IO211PB6F19	55
IO212NB6F19	52
IO212PB6F19	53
IO223NB6F20	48
IO223PB6F20	49
IO224NB6F20	46
IO224PB6F20	47
Bank 7	
IO225NB7F21	40
IO225PB7F21	41
IO226NB7F21	42
IO226PB7F21	43
IO237NB7F22	34
IO237PB7F22	35
IO238NB7F22	36

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
IO238PB7F22	37
IO240NB7F22	30
IO240PB7F22	31
IO241NB7F22	28
IO241PB7F22	29
IO242NB7F22	24
IO242PB7F22	25
IO244NB7F22	22
IO244PB7F22	23
IO245NB7F22	18
IO245PB7F22	19
IO246NB7F22	16
IO246PB7F22	17
IO249NB7F23	12
IO249PB7F23	13
IO250NB7F23	10
IO250PB7F23	11
IO256NB7F23	4
IO256PB7F23	5
IO257NB7F23	6
IO257PB7F23	7
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
GND	334
GND	340
GND	345
GND	352
NC	91
NC	124
NC	125
NC	126
NC	127
NC	130
NC	131
NC	138
NC	139
NC	140
NC	141
NC	174
NC	268
NC	301
NC	302
NC	303
NC	304
NC	307
NC	308
NC	315
NC	316
NC	317
NC	318
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
V_{CCA}	3

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
V_{CCA}	14
V_{CCA}	32
V_{CCA}	56
V_{CCA}	74
V_{CCA}	87
V_{CCA}	102
V_{CCA}	114
V_{CCA}	150
V_{CCA}	162
V_{CCA}	175
V_{CCA}	191
V_{CCA}	209
V_{CCA}	233
V_{CCA}	251
V_{CCA}	263
V_{CCA}	279
V_{CCA}	291
V_{CCA}	329
V_{CCA}	339
V_{CCDA}	2
V_{CCDA}	44
V_{CCDA}	90
V_{CCDA}	116
V_{CCDA}	117
V_{CCDA}	132
V_{CCDA}	148
V_{CCDA}	149
V_{CCDA}	178
V_{CCDA}	221
V_{CCDA}	266
V_{CCDA}	293
V_{CCDA}	294
V_{CCDA}	309
V_{CCDA}	327
V_{CCDA}	328
V_{CCDA}	346
$V_{CCI}B0$	321

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
$V_{CCI}B0$	333
$V_{CCI}B0$	344
$V_{CCI}B1$	273
$V_{CCI}B1$	285
$V_{CCI}B1$	297
$V_{CCI}B2$	227
$V_{CCI}B2$	239
$V_{CCI}B2$	245
$V_{CCI}B2$	257
$V_{CCI}B3$	185

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
$V_{CCI}B3$	197
$V_{CCI}B3$	203
$V_{CCI}B3$	215
$V_{CCI}B4$	144
$V_{CCI}B4$	156
$V_{CCI}B4$	168
$V_{CCI}B5$	96
$V_{CCI}B5$	108
$V_{CCI}B5$	120

352-Pin CQFP	
RTAX1000S/SL Function	**Pin Number**
$V_{CCI}B6$	50
$V_{CCI}B6$	62
$V_{CCI}B6$	68
$V_{CCI}B6$	80
$V_{CCI}B7$	8
$V_{CCI}B7$	20
$V_{CCI}B7$	26
$V_{CCI}B7$	38
V_{PUMP}	267

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
Bank 0	
IO01NB0F0	341
IO01PB0F0	342
IO02PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO05NB0F0	335
IO05PB0F0	336
IO08NB0F0	331
IO08PB0F0	332
IO37NB0F3	325
IO37PB0F3	326
IO38NB0F3	323
IO38PB0F3	324
IO41NB0F3/HCLKAN	319
IO41PB0F3/HCLKAP	320
IO42NB0F3/HCLKBN	313
IO42PB0F3/HCLKBP	314
Bank 1	
IO43NB1F4/HCLKCN	305
IO43PB1F4/HCLKCP	306
IO44NB1F4/HCLKDN	299
IO44PB1F4/HCLKDP	300
IO48NB1F4	295
IO48PB1F4	296
IO65NB1F6	283
IO65PB1F6	284
IO66NB1F6	289
IO66PB1F6	290
IO68NB1F6	287
IO68PB1F6	288
IO69NB1F6	275
IO69PB1F6	276
IO70NB1F6	281
IO70PB1F6	282
IO71NB1F6	277
IO71PB1F6	278

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
IO73NB1F6	269
IO73PB1F6	270
IO74NB1F6	271
IO74PB1F6	272
Bank 2	
IO87NB2F8	261
IO87PB2F8	262
IO88NB2F8	255
IO88PB2F8	256
IO89NB2F8	259
IO89PB2F8	260
IO91NB2F8	253
IO91PB2F8	254
IO99NB2F9	249
IO99PB2F9	250
IO100NB2F9	247
IO100PB2F9	248
IO107NB2F10	243
IO107PB2F10	244
IO110NB2F10	241
IO110PB2F10	242
IO111NB2F10	237
IO111PB2F10	238
IO112NB2F10	235
IO112PB2F10	236
IO113NB2F10	231
IO113PB2F10	232
IO114NB2F10	229
IO114PB2F10	230
IO115NB2F10	225
IO115PB2F10	226
IO117NB2F10	223
IO117PB2F10	224
Bank 3	
IO129NB3F12	219
IO129PB3F12	220
IO132NB3F12	217

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
IO132PB3F12	218
IO137NB3F12	213
IO137PB3F12	214
IO139NB3F13	211
IO139PB3F13	212
IO141NB3F13	205
IO141PB3F13	206
IO142NB3F13	207
IO142PB3F13	208
IO145NB3F13	199
IO145PB3F13	200
IO146NB3F13	201
IO146PB3F13	202
IO147NB3F13	193
IO147PB3F13	194
IO148NB3F13	195
IO148PB3F13	196
IO149NB3F13	189
IO149PB3F13	190
IO161NB3F15	183
IO161PB3F15	184
IO163NB3F15	187
IO163PB3F15	188
IO165NB3F15	181
IO165PB3F15	182
IO167NB3F15	179
IO167PB3F15	180
Bank 4	
IO181NB4F17	172
IO181PB4F17	173
IO182NB4F17	170
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88

352-Pin CQFP	
RTAX2000S/SL Function	Pin Number
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330

352-Pin CQFP	
RTAX2000S/SL Function	Pin Number
GND	334
GND	340
GND	345
GND	352
NC	124
NC	125
NC	126
NC	127
NC	138
NC	139
NC	140
NC	141
NC	301
NC	302
NC	303
NC	304
NC	315
NC	316
NC	317
NC	318
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
V_{CCA}	3
V_{CCA}	14
V_{CCA}	32
V_{CCA}	56
V_{CCA}	74
V_{CCA}	87
V_{CCA}	102
V_{CCA}	114

352-Pin CQFP	
RTAX2000S/SL Function	Pin Number
V_{CCA}	150
V_{CCA}	162
V_{CCA}	175
V_{CCA}	191
V_{CCA}	209
V_{CCA}	233
V_{CCA}	251
V_{CCA}	263
V_{CCA}	279
V_{CCA}	291
V_{CCA}	329
V_{CCA}	339
V_{CCDA}	2
V_{CCDA}	44
V_{CCDA}	90
V_{CCDA}	91
V_{CCDA}	116
V_{CCDA}	117
V_{CCDA}	130
V_{CCDA}	131
V_{CCDA}	132
V_{CCDA}	148
V_{CCDA}	149
V_{CCDA}	174
V_{CCDA}	178
V_{CCDA}	221
V_{CCDA}	266
V_{CCDA}	268
V_{CCDA}	293
V_{CCDA}	294
V_{CCDA}	307
V_{CCDA}	308
V_{CCDA}	309
V_{CCDA}	327
V_{CCDA}	328
V_{CCDA}	346
$V_{CCI}B0$	321

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B0$	333
$V_{CCI}B0$	344
$V_{CCI}B1$	273
$V_{CCI}B1$	285
$V_{CCI}B1$	297
$V_{CCI}B2$	227
$V_{CCI}B2$	239
$V_{CCI}B2$	245
$V_{CCI}B2$	257
$V_{CCI}B3$	185

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B3$	197
$V_{CCI}B3$	203
$V_{CCI}B3$	215
$V_{CCI}B4$	144
$V_{CCI}B4$	156
$V_{CCI}B4$	168
$V_{CCI}B5$	96
$V_{CCI}B5$	108
$V_{CCI}B5$	120

352-Pin CQFP	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B6$	50
$V_{CCI}B6$	62
$V_{CCI}B6$	68
$V_{CCI}B6$	80
$V_{CCI}B7$	8
$V_{CCI}B7$	20
$V_{CCI}B7$	26
$V_{CCI}B7$	38
V_{PUMP}	267

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
Bank 0	
IO02NB0F0	341
IO02PB0F0	342
IO03PB0F0	343
IO05NB0F0	337
IO05PB0F0	338
IO06NB0F0	335
IO06PB0F0	336
IO07NB0F0	331
IO07PB0F0	332
IO11NB0F0	329
IO11PB0F0	330
IO50NB0F4/HCLKAN	317
IO50PB0F4/HCLKAP	318
IO51NB0F4/HCLKBN	313
IO51PB0F4/HCLKBP	314
Bank 1	
IO52NB1F6/HCLKCN	303
IO52PB1F6/HCLKCP	304
IO53NB1F6/HCLKDN	299
IO53PB1F6/HCLKDP	300
IO94NB1F10	287
IO94PB1F10	288
IO97NB1F10	281
IO97PB1F10	282
IO98NB1F10	285
IO98PB1F10	286
IO99NB1F10	275
IO99PB1F10	276
IO100NB1F10	279
IO100PB1F10	280
IO102NB1F10	273
IO102PB1F10	274
IO103NB1F10	269
IO103PB1F10	270
Bank 2	
IO104NB2F12	259

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
IO104PB2F12	260
IO106NB2F12	253
IO106PB2F12	254
IO107NB2F12	257
IO107PB2F12	258
IO111NB2F12	251
IO111PB2F12	252
IO139NB2F16	241
IO139PB2F16	242
IO140NB2F16	245
IO140PB2F16	246
IO141NB2F16	235
IO141PB2F16	236
IO142NB2F16	239
IO142PB2F16	240
IO143NB2F16	229
IO143PB2F16	230
IO144NB2F16	233
IO144PB2F16	234
IO145NB2F16	223
IO145PB2F16	224
IO146NB2F16	227
IO146PB2F16	228
Bank 3	
IO175NB3F20	213
IO175PB3F20	214
IO176NB3F20	217
IO176PB3F20	218
IO177NB3F20	207
IO177PB3F20	208
IO178NB3F20	211
IO178PB3F20	212
IO179NB3F20	205
IO179PB3F20	206
IO181NB3F20	201
IO181PB3F20	202
IO182NB3F20	199

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
IO182PB3F20	200
IO183NB3F20	195
IO183PB3F20	196
IO203NB3F23	189
IO203PB3F23	190
IO204NB3F23	183
IO204PB3F23	184
IO206NB3F23	187
IO206PB3F23	188
IO209NB3F23	181
IO209PB3F23	182
Bank 4	
IO210NB4F24	167
IO210PB4F24	168
IO211NB4F24	173
IO213NB4F24	171
IO213PB4F24	172
IO214NB4F24	161
IO214PB4F24	162
IO215NB4F24	165
IO215PB4F24	166
IO216NB4F24	155
IO216PB4F24	156
IO217NB4F24	159
IO217PB4F24	160
IO219NB4F24	153
IO219PB4F24	154
IO260NB4F28/CLKEN	141
IO260PB4F28/CLKEP	142
IO261NB4F28/CLKFN	137
IO261PB4F28/CLKFP	138
Bank 5	
IO262NB5F30/CLKGN	127
IO262PB5F30/CLKGP	128
IO263NB5F30/CLKHN	123
IO263PB5F30/CLKHP	124
IO304NB5F34	111

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
IO304PB5F34	112
IO305NB5F34	109
IO305PB5F34	110
IO307NB5F34	103
IO307PB5F34	104
IO308NB5F34	105
IO308PB5F34	106
IO309NB5F34	97
IO309PB5F34	98
IO310NB5F34	99
IO310PB5F34	100
IO312NB5F34	93
IO312PB5F34	94
IO313NB5F34	92
Bank 6	
IO314PB6F36	84
IO316NB6F36	82
IO316PB6F36	83
IO317NB6F36	78
IO317PB6F36	79
IO319NB6F36	76
IO319PB6F36	77
IO349NB6F40	66
IO349PB6F40	67
IO350NB6F40	70
IO350PB6F40	71
IO351NB6F40	60
IO351PB6F40	61
IO352NB6F40	64
IO352PB6F40	65
IO353NB6F40	54
IO353PB6F40	55
IO354NB6F40	58
IO354PB6F40	59
IO355NB6F40	48
IO355PB6F40	49
IO356NB6F40	52

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
IO356PB6F40	53
Bank 7	
IO385NB7F44	42
IO385PB7F44	43
IO386NB7F44	38
IO386PB7F44	39
IO387NB7F44	36
IO387PB7F44	37
IO388NB7F44	32
IO388PB7F44	33
IO389NB7F44	30
IO389PB7F44	31
IO391NB7F44	26
IO391PB7F44	27
IO392NB7F44	24
IO392PB7F44	25
IO393NB7F44	20
IO393PB7F44	21
IO413NB7F47	14
IO413PB7F47	15
IO414NB7F47	8
IO414PB7F47	9
IO416NB7F47	12
IO416PB7F47	13
IO419NB7F47	6
IO419PB7F47	7
Dedicated I/O	
GND	1
GND	5
GND	11
GND	17
GND	19
GND	23
GND	29
GND	35
GND	41
GND	45

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
GND	47
GND	51
GND	57
GND	63
GND	69
GND	73
GND	75
GND	81
GND	86
GND	88
GND	89
GND	96
GND	102
GND	108
GND	117
GND	119
GND	126
GND	132
GND	134
GND	140
GND	147
GND	149
GND	158
GND	164
GND	170
GND	176
GND	177
GND	180
GND	186
GND	192
GND	194
GND	198
GND	204
GND	210
GND	216
GND	220
GND	222

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
GND	226
GND	232
GND	238
GND	244
GND	248
GND	250
GND	256
GND	262
GND	264
GND	265
GND	272
GND	278
GND	284
GND	293
GND	295
GND	302
GND	308
GND	310
GND	316
GND	323
GND	325
GND	334
GND	340
GND	345
GND	352
PRA	312
PRB	311
PRC	136
PRD	135
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
V_{CCA}	3
V_{CCA}	4
V_{CCA}	18

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
V_{CCA}	34
V_{CCA}	44
V_{CCA}	56
V_{CCA}	72
V_{CCA}	85
V_{CCA}	87
V_{CCA}	101
V_{CCA}	116
V_{CCA}	129
V_{CCA}	131
V_{CCA}	148
V_{CCA}	163
V_{CCA}	175
V_{CCA}	179
V_{CCA}	193
V_{CCA}	209
V_{CCA}	219
V_{CCA}	231
V_{CCA}	247
V_{CCA}	261
V_{CCA}	263
V_{CCA}	277
V_{CCA}	292
V_{CCA}	305
V_{CCA}	307
V_{CCA}	324
V_{CCA}	339
V_{CCDA}	2
V_{CCDA}	16
V_{CCDA}	46
V_{CCDA}	74
V_{CCDA}	90
V_{CCDA}	91
V_{CCDA}	113
V_{CCDA}	114
V_{CCDA}	115
V_{CCDA}	118

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
V_{CCDA}	120
V_{CCDA}	121
V_{CCDA}	122
V_{CCDA}	130
V_{CCDA}	133
V_{CCDA}	143
V_{CCDA}	144
V_{CCDA}	145
V_{CCDA}	146
V_{CCDA}	150
V_{CCDA}	151
V_{CCDA}	152
V_{CCDA}	174
V_{CCDA}	178
V_{CCDA}	191
V_{CCDA}	221
V_{CCDA}	249
V_{CCDA}	266
V_{CCDA}	268
V_{CCDA}	289
V_{CCDA}	290
V_{CCDA}	291
V_{CCDA}	294
V_{CCDA}	296
V_{CCDA}	297
V_{CCDA}	298
V_{CCDA}	306
V_{CCDA}	309
V_{CCDA}	319
V_{CCDA}	320
V_{CCDA}	321
V_{CCDA}	322
V_{CCDA}	326
V_{CCDA}	327
V_{CCDA}	328
V_{CCDA}	346
$V_{CCI}B0$	315

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
$V_{CCI}B0$	333
$V_{CCI}B0$	344
$V_{CCI}B1$	271
$V_{CCI}B1$	283
$V_{CCI}B1$	301
$V_{CCI}B2$	225
$V_{CCI}B2$	237
$V_{CCI}B2$	243
$V_{CCI}B2$	255
$V_{CCI}B3$	185

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
$V_{CCI}B3$	197
$V_{CCI}B3$	203
$V_{CCI}B3$	215
$V_{CCI}B4$	139
$V_{CCI}B4$	157
$V_{CCI}B4$	169
$V_{CCI}B5$	95
$V_{CCI}B5$	107
$V_{CCI}B5$	125

352-Pin CQFP	
RTAX4000S/SL Function	**Pin Number**
$V_{CCI}B6$	50
$V_{CCI}B6$	62
$V_{CCI}B6$	68
$V_{CCI}B6$	80
$V_{CCI}B7$	10
$V_{CCI}B7$	22
$V_{CCI}B7$	28
$V_{CCI}B7$	40
V_{PUMP}	267

624-Pin CCGA/LGA

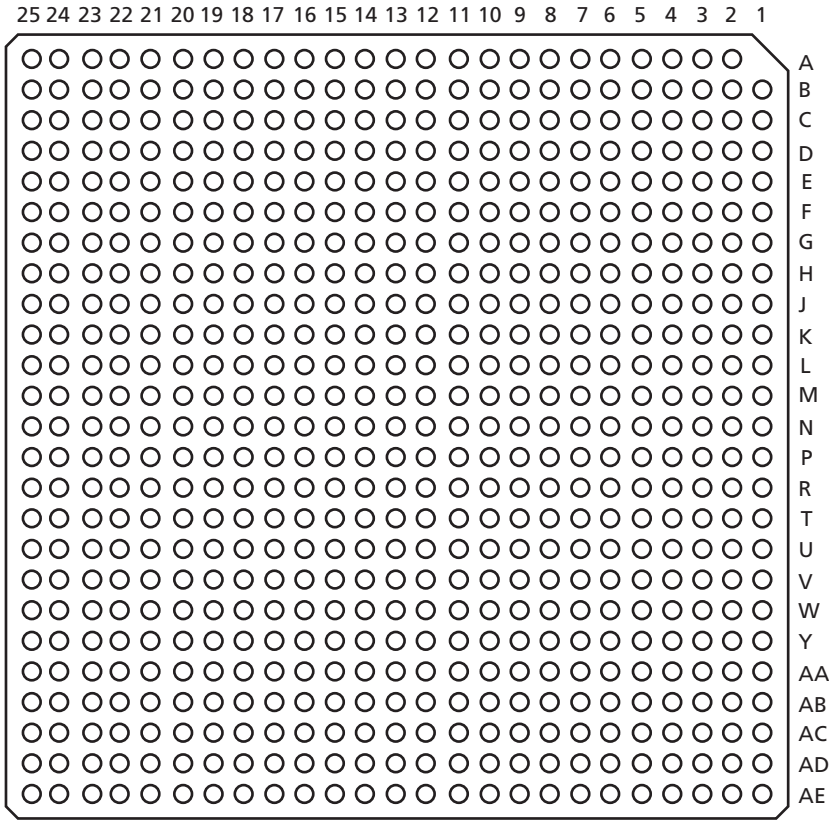


Figure 3-4 • **624-Pin CCGA/LGA (Bottom View)**

Note:

The 624-pin CCGA pin assignments for RTAX250S/SL, RTAX1000S/SL and RTAX2000S/SL are compatible except for the following pins.

Table 3-2 • **Compatibility Table for the CGA/LGA 624 Package**

	RTAX250S/SL	**RTAX1000S/SL**	**RTAX2000S/SL**
RTAX250S/SL	NA	A12, AD11, AE17, B15, D13	A12, A14, AA20, AB13, AD11, AD4, AE12, B15, D13, F21, G10
RTAX1000S/SL	A12, AD11, AE17, B15, D13	NA	A14, AA20, AB13, AD4, AE12, F21, G10
RTAX2000S/SL	A12, A14, AA20, AB13, AD11, AD4, AE12, B15, D13, F21, G10	A14, AA20, AB13, AD4, AE12, F21, G10	NA

Where exceptions occur, the smaller density devices have those pins designated as No Connects (NC). Customers are therefore recommended to layout their board targeting the larger density device, in order to preserve interchangeability between the two devices. Note: RTAX4000S is not pin compatible with any of the smaller density devices.

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
Bank 0	
IO00NB0F0	C9
IO00PB0F0	C8
IO01NB0F0	B5
IO01PB0F0	B4
IO02NB0F0	D10
IO02PB0F0	D9
IO03NB0F0	A5
IO03PB0F0	A4
IO04NB0F0	H8
IO04PB0F0	H7
IO05NB0F0	A7
IO05PB0F0	A6
IO06NB0F0	H10
IO06PB0F0	H9
IO07NB0F0	B11
IO07PB0F0	B10
IO08NB0F0	J8
IO08PB0F0	J7
IO09NB0F0	A9
IO09PB0F0	B9
IO12NB0F0/HCLKAN	G13
IO12PB0F0/HCLKAP	G12
IO13NB0F0/HCLKBN	C13
IO13PB0F0/HCLKBP	C12
Bank 1	
IO16NB1F1	D14
IO16PB1F1	C14
IO17NB1F1	A16
IO17PB1F1	A15
IO18NB1F1	H20
IO18PB1F1	H19
IO19NB1F1	B17
IO19PB1F1	B16
IO20NB1F1	D16
IO20PB1F1	D15
IO21NB1F1	A20

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
IO21PB1F1	A19
IO22NB1F1	D18
IO22PB1F1	D17
IO23NB1F1	A22
IO23PB1F1	A21
IO24NB1F1	G17
IO24PB1F1	H17
IO25NB1F1	C21
IO25PB1F1	C20
IO26NB1F1	C19
IO26PB1F1	C18
IO27NB1F1	D20
IO27PB1F1	D19
IO14NB1F1/HCLKCN	G15
IO14PB1F1/HCLKCP	G14
IO15NB1F1/HCLKDN	B14
IO15PB1F1/HCLKDP	B13
Bank 2	
IO28NB2F2	J22
IO28PB2F2	H22
IO29NB2F2	L18
IO29PB2F2	K18
IO30NB2F2	F23
IO30PB2F2	E23
IO31NB2F2	J21
IO31PB2F2	J20
IO32NB2F2	E25
IO32PB2F2	D25
IO33NB2F2	M19
IO33PB2F2	M18
IO34NB2F2	H23
IO34PB2F2	G23
IO35NB2F2	L22
IO35PB2F2	K22
IO36NB2F2	G25
IO36PB2F2	F25
IO37NB2F2	L24

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
IO37PB2F2	K24
IO38NB2F2	J24
IO38PB2F2	H24
IO39NB2F2	N22
IO39PB2F2	M22
IO40NB2F2	N24
IO40PB2F2	M24
IO41NB2F2	N19
IO41PB2F2	N18
IO42NB2F2	L25
IO42PB2F2	K25
IO43NB2F2	N23
IO43PB2F2	M23
IO44NB2F2	N25
IO44PB2F2	M25
Bank 3	
IO45NB3F3	R22
IO45PB3F3	P22
IO46NB3F3	R25
IO46PB3F3	P25
IO47NB3F3	R23
IO47PB3F3	P23
IO48NB3F3	Y25
IO48PB3F3	W25
IO49NB3F3	U24
IO49PB3F3	U23
IO50NB3F3	T24
IO50PB3F3	R24
IO51NB3F3	Y23
IO51PB3F3	AA23
IO52NB3F3	V23
IO52PB3F3	V24
IO53NB3F3	P20
IO53PB3F3	P19
IO54NB3F3	U25
IO54PB3F3	T25
IO55NB3F3	V22

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
IO55PB3F3	U22
IO56NB3F3	AA24
IO56PB3F3	Y24
IO57NB3F3	V20
IO57PB3F3	U20
IO58NB3F3	AB25
IO58PB3F3	AA25
IO59NB3F3	Y22
IO59PB3F3	Y21
IO60NB3F3	W22
IO60PB3F3	W23
IO61NB3F3	T18
IO61PB3F3	R18
Bank 4	
IO62NB4F4	V19
IO62PB4F4	W19
IO63NB4F4	AE19
IO63PB4F4	AE20
IO64NB4F4	W18
IO64PB4F4	V18
IO65NB4F4	AC20
IO65PB4F4	AC21
IO66NB4F4	AD14
IO66PB4F4	AC14
IO67NB4F4	AD21
IO67PB4F4	AD22
IO68NB4F4	AD15
IO68PB4F4	AD16
IO69NB4F4	AD19
IO69PB4F4	AD20
IO70NB4F4	AB14
IO70PB4F4	AB15
IO71NB4F4	AD17
IO71PB4F4	AD18
IO72NB4F4	V15
IO72PB4F4	V16
IO73NB4F4	AE15

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
IO73PB4F4	AE16
IO74NB4F4/CLKEN	W14
IO74PB4F4/CLKEP	W15
IO75NB4F4/CLKFN	AC13
IO75PB4F4/CLKFP	AD13
Bank 5	
IO78NB5F5	AE10
IO78PB5F5	AE11
IO79NB5F5	AD9
IO79PB5F5	AD10
IO80NB5F5	V9
IO80PB5F5	V10
IO81NB5F5	AD7
IO81PB5F5	AD8
IO82NB5F5	AB10
IO82PB5F5	AB11
IO83NB5F5	AE6
IO83PB5F5	AE7
IO84NB5F5	AB8
IO84PB5F5	AC8
IO85NB5F5	AE4
IO85PB5F5	AE5
IO86NB5F5	U13
IO86PB5F5	V13
IO87NB5F5	AC5
IO87PB5F5	AC6
IO88NB5F5	Y7
IO88PB5F5	W7
IO89NB5F5	AB7
IO89PB5F5	AC7
IO76NB5F5/CLKGN	W13
IO76PB5F5/CLKGP	Y13
IO77NB5F5/CLKHN	AC12
IO77PB5F5/CLKHP	AD12
Bank 6	
IO90NB6F6	Y3
IO90PB6F6	AA3

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
IO91NB6F6	U4
IO91PB6F6	V4
IO92NB6F6	AA1
IO92PB6F6	AB1
IO93NB6F6	W2
IO93PB6F6	Y2
IO94NB6F6	V3
IO94PB6F6	W3
IO95NB6F6	R4
IO95PB6F6	T4
IO96NB6F6	W1
IO96PB6F6	Y1
IO97NB6F6	Y5
IO97PB6F6	W5
IO98NB6F6	T2
IO98PB6F6	U2
IO99NB6F6	N3
IO99PB6F6	P3
IO100NB6F6	T1
IO100PB6F6	U1
IO101NB6F6	N4
IO101PB6F6	P4
IO102NB6F6	P2
IO102PB6F6	R2
IO103NB6F6	R8
IO103PB6F6	T8
IO104NB6F6	P1
IO104PB6F6	R1
IO105NB6F6	M2
IO105PB6F6	N2
IO106NB6F6	M1
IO106PB6F6	N1
Bank 7	
IO107NB7F7	H4
IO107PB7F7	J4
IO108NB7F7	K1
IO108PB7F7	L1

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
IO109NB7F7	L3
IO109PB7F7	M3
IO10NB0F0	D12
IO10PB0F0	D11
IO110NB7F7	J2
IO110PB7F7	J1
IO111NB7F7	N10
IO111PB7F7	N9
IO112NB7F7	K2
IO112PB7F7	L2
IO113NB7F7	K8
IO113PB7F7	L8
IO114NB7F7	F1
IO114PB7F7	G1
IO115NB7F7	J6
IO115PB7F7	J5
IO116NB7F7	H3
IO116PB7F7	H2
IO117NB7F7	K4
IO117PB7F7	L4
IO118NB7F7	E2
IO118PB7F7	F2
IO119NB7F7	M9
IO119PB7F7	M8
IO11NB0F0	A11
IO11PB0F0	A10
IO120NB7F7	D1
IO120PB7F7	E1
IO121NB7F7	F3
IO121PB7F7	E3
IO122NB7F7	G4
IO122PB7F7	G3
IO123NB7F7	H5
IO123PB7F7	H6
Dedicated IO	
GND	K5
GND	T5

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
GND	V5
GND	AA10
GND	AA16
GND	AA18
GND	T21
GND	K21
GND	H21
GND	E16
GND	E10
GND	E8
GND	A18
GND	A2
GND	A24
GND	A25
GND	A8
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E21
GND	E5
GND	H1
GND	H25
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	Pin Number
GND	T23
GND	T3
GND	V1
GND	V25
NC	A12
NC	A14
NC	A17
NC	AA11
NC	AA12
NC	AA14
NC	AA17
NC	AA19
NC	AA2
NC	AA20
NC	AA6
NC	AA8
NC	AA9
NC	AB13
NC	AB16
NC	AB17
NC	AB18
NC	AB19
NC	AB2
NC	AB24
NC	AB6
NC	AB9
NC	AC15
NC	AC17
NC	AC18
NC	AC19
NC	AC9
NC	AD11
NC	AD4
NC	AD5
NC	AD6
NC	AE12
NC	AE14

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	Pin Number
NC	AE17
NC	AE21
NC	AE22
NC	AE9
NC	B12
NC	B15
NC	B18
NC	B19
NC	B20
NC	B21
NC	B22
NC	B6
NC	B7
NC	B8
NC	C11
NC	C17
NC	C7
NC	D13
NC	D2
NC	D24
NC	D7
NC	D8
NC	E11
NC	E12
NC	E14
NC	E15
NC	E17
NC	E18
NC	E24
NC	E7
NC	E9
NC	F10
NC	F11
NC	F12
NC	F14
NC	F15
NC	F16

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	Pin Number
NC	F17
NC	F18
NC	F19
NC	F20
NC	F21
NC	F24
NC	F7
NC	F8
NC	F9
NC	G10
NC	G11
NC	G16
NC	G18
NC	G19
NC	G2
NC	G20
NC	G21
NC	G22
NC	G24
NC	G6
NC	G7
NC	G8
NC	G9
NC	H11
NC	H12
NC	H13
NC	H14
NC	H15
NC	H16
NC	H18
NC	J12
NC	J13
NC	J14
NC	J18
NC	J19
NC	J23
NC	J25

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
NC	J3
NC	K13
NC	K19
NC	K20
NC	K6
NC	K7
NC	L19
NC	L20
NC	L21
NC	L23
NC	L5
NC	L6
NC	L7
NC	M17
NC	M20
NC	M21
NC	M4
NC	M5
NC	M6
NC	M7
NC	N16
NC	N17
NC	N20
NC	N6
NC	N7
NC	N8
NC	P17
NC	P18
NC	P21
NC	P24
NC	P5
NC	P6
NC	P7
NC	P8
NC	P9
NC	R19
NC	R20

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
NC	R21
NC	R3
NC	R5
NC	R6
NC	R7
NC	T13
NC	T19
NC	T20
NC	T22
NC	T6
NC	T7
NC	U12
NC	U14
NC	U18
NC	U19
NC	U21
NC	U3
NC	U5
NC	U6
NC	U7
NC	U8
NC	V11
NC	V12
NC	V14
NC	V17
NC	V2
NC	V21
NC	V6
NC	V7
NC	V8
NC	W10
NC	W11
NC	W12
NC	W16
NC	W17
NC	W20
NC	W24

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
NC	W4
NC	W6
NC	W8
NC	W9
NC	Y10
NC	Y11
NC	Y12
NC	Y14
NC	Y15
NC	Y16
NC	Y17
NC	Y18
NC	Y19
NC	Y20
NC	Y6
NC	Y8
NC	Y9
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5
TDI	C5
TDO	F6
TMS	D6
TRST	E6
V_{CCA}	F4
V_{CCA}	Y4
V_{CCA}	AB20
V_{CCA}	F22
V_{CCA}	J17
V_{CCA}	J9
V_{CCA}	K10
V_{CCA}	K11
V_{CCA}	K15
V_{CCA}	K16
V_{CCA}	L10

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
V_{CCA}	L16
V_{CCA}	R10
V_{CCA}	R16
V_{CCA}	T10
V_{CCA}	T11
V_{CCA}	T15
V_{CCA}	T16
V_{CCA}	U17
V_{CCA}	U9
V_{CCDA}	G5
V_{CCDA}	N5
V_{CCDA}	AA7
V_{CCDA}	AC11
V_{CCDA}	AA13
V_{CCDA}	AA15
V_{CCDA}	W21
V_{CCDA}	N21
V_{CCDA}	E19
V_{CCDA}	C15
V_{CCDA}	E13
V_{CCDA}	C6
$V_{CCI}B0$	A3
$V_{CCI}B0$	B3
$V_{CCI}B0$	C4
$V_{CCI}B0$	D5
$V_{CCI}B0$	J10
$V_{CCI}B0$	J11
$V_{CCI}B0$	K12
$V_{CCI}B1$	A23
$V_{CCI}B1$	B23
$V_{CCI}B1$	C22
$V_{CCI}B1$	D21
$V_{CCI}B1$	J15
$V_{CCI}B1$	J16
$V_{CCI}B1$	K14
$V_{CCI}B2$	C24
$V_{CCI}B2$	C25

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
$V_{CCI}B2$	D23
$V_{CCI}B2$	E22
$V_{CCI}B2$	K17
$V_{CCI}B2$	L17
$V_{CCI}B2$	M16
$V_{CCI}B3$	AA22
$V_{CCI}B3$	AB23
$V_{CCI}B3$	AC24
$V_{CCI}B3$	AC25
$V_{CCI}B3$	P16
$V_{CCI}B3$	R17
$V_{CCI}B3$	T17
$V_{CCI}B4$	AB21
$V_{CCI}B4$	AC22
$V_{CCI}B4$	AD23
$V_{CCI}B4$	AE23
$V_{CCI}B4$	T14
$V_{CCI}B4$	U15
$V_{CCI}B4$	U16
$V_{CCI}B5$	AB5
$V_{CCI}B5$	AC4
$V_{CCI}B5$	AD3
$V_{CCI}B5$	AE3
$V_{CCI}B5$	T12
$V_{CCI}B5$	U10
$V_{CCI}B5$	U11
$V_{CCI}B6$	AA4
$V_{CCI}B6$	AB3
$V_{CCI}B6$	AC1
$V_{CCI}B6$	AC2
$V_{CCI}B6$	P10
$V_{CCI}B6$	R9
$V_{CCI}B6$	T9
$V_{CCI}B7$	C1
$V_{CCI}B7$	C2
$V_{CCI}B7$	D3
$V_{CCI}B7$	E4

624-Pin CCGA/LGA	
RTAX250S/SL Pin Function	**Pin Number**
$V_{CCI}B7$	K9
$V_{CCI}B7$	L9
$V_{CCI}B7$	M10
V_{PUMP}	E20

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
Bank 0	
IO00NB0F0	F8
IO00PB0F0	F7
IO02NB0F0	G7
IO02PB0F0	G6
IO04NB0F0	E9
IO04PB0F0	D8
IO06NB0F0	G9
IO06PB0F0	G8
IO07PB0F0	B6
IO08NB0F0	F10
IO08PB0F0	F9
IO09PB0F0	C7
IO10NB0F0	H8
IO10PB0F0	H7
IO11NB0F0	D10
IO11PB0F0	D9
IO12NB0F1	B5
IO12PB0F1	B4
IO13NB0F1	A7
IO13PB0F1	A6
IO14NB0F1	C9
IO14PB0F1	C8
IO15PB0F1	B7
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	A9
IO17PB0F1	B9
IO18NB0F1	D12
IO18PB0F1	D11
IO20NB0F1	B11
IO20PB0F1	B10
IO21NB0F1	A11
IO21PB0F1	A10
IO22NB0F2	H10
IO22PB0F2	H9

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO23NB0F2	E11
IO23PB0F2	F11
IO24NB0F2	D7
IO24PB0F2	E7
IO25PB0F2	B12
IO26NB0F2	H11
IO26PB0F2	G11
IO27NB0F2	C11
IO27PB0F2	B8
IO28NB0F2	J13
IO28PB0F2	K13
IO29NB0F2	J8
IO29PB0F2	J7
IO30NB0F2/HCLKAN	G13
IO30PB0F2/HCLKAP	G12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	C12
Bank 1	
IO32NB1F3/HCLKCN	G15
IO32PB1F3/HCLKCP	G14
IO33NB1F3/HCLKDN	B14
IO33PB1F3/HCLKDP	B13
IO34NB1F3	G16
IO34PB1F3	H16
IO35NB1F3	C17
IO35PB1F3	B18
IO36NB1F3	H18
IO36PB1F3	H15
IO37NB1F3	H13
IO38NB1F3	E15
IO38PB1F3	F15
IO39NB1F3	D14
IO39PB1F3	C14
IO40NB1F3	D16
IO40PB1F3	D15
IO41NB1F4	F16

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO42NB1F4	G21
IO42PB1F4	G20
IO43NB1F4	A16
IO43PB1F4	A15
IO44NB1F4	A20
IO44PB1F4	A19
IO45NB1F4	B17
IO45PB1F4	B16
IO46NB1F4	G17
IO46PB1F4	H17
IO47NB1F4	A17
IO48NB1F4	C19
IO48PB1F4	C18
IO49NB1F4	B20
IO49PB1F4	B19
IO50NB1F4	H20
IO50PB1F4	H19
IO51NB1F4	A22
IO51PB1F4	A21
IO52NB1F4	C21
IO52PB1F4	C20
IO53NB1F4	B22
IO53PB1F4	B21
IO54NB1F5	J18
IO54PB1F5	J19
IO55NB1F5	D18
IO55PB1F5	D17
IO56NB1F5	F20
IO56PB1F5	F19
IO58NB1F5	E17
IO58PB1F5	F17
IO60NB1F5	D20
IO60PB1F5	D19
IO62NB1F5	E18
IO62PB1F5	F18
IO63NB1F5	G19

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO63PB1F5	G18
Bank 2	
IO64NB2F6	M17
IO64PB2F6	G22
IO65NB2F6	J21
IO65PB2F6	J20
IO66NB2F6	L23
IO66PB2F6	K20
IO67NB2F6	F23
IO67PB2F6	E23
IO68NB2F6	L18
IO68PB2F6	K18
IO70NB2F6	E24
IO70PB2F6	D24
IO71NB2F6	H23
IO71PB2F6	G23
IO72NB2F6	L19
IO72PB2F6	K19
IO74NB2F7	J22
IO74PB2F7	H22
IO75NB2F7	N23
IO75PB2F7	M23
IO76NB2F7	N17
IO76PB2F7	N16
IO77NB2F7	L22
IO77PB2F7	K22
IO78NB2F7	M19
IO78PB2F7	M18
IO79NB2F7	N19
IO79PB2F7	N18
IO80NB2F7	L21
IO80PB2F7	L20
IO82NB2F7	P18
IO82PB2F7	P17
IO83NB2F7	N22
IO83PB2F7	M22

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO84NB2F7	M20
IO84PB2F7	M21
IO86NB2F8	E25
IO86PB2F8	D25
IO87NB2F8	L24
IO87PB2F8	K24
IO88NB2F8	G24
IO88PB2F8	F24
IO89NB2F8	J25
IO90NB2F8	G25
IO90PB2F8	F25
IO91NB2F8	L25
IO91PB2F8	K25
IO92NB2F8	J24
IO92PB2F8	H24
IO93PB2F8	J23
IO94NB2F8	N24
IO94PB2F8	M24
IO95NB2F8	N25
IO95PB2F8	M25
Bank 3	
IO96NB3F9	T18
IO96PB3F9	R18
IO97NB3F9	N20
IO97PB3F9	P24
IO98NB3F9	P20
IO98PB3F9	P19
IO99NB3F9	P21
IO100NB3F9	T22
IO100PB3F9	W24
IO101NB3F9	R22
IO101PB3F9	P22
IO102NB3F9	U19
IO102PB3F9	T19
IO104NB3F9	V20
IO104PB3F9	U20

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO105NB3F9	R23
IO105PB3F9	P23
IO106NB3F9	R19
IO106PB3F9	R20
IO107NB3F10	AB24
IO108NB3F10	R25
IO108PB3F10	P25
IO109NB3F10	U25
IO109PB3F10	T25
IO110NB3F10	U24
IO110PB3F10	U23
IO112NB3F10	T24
IO112PB3F10	R24
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V23
IO114PB3F10	V24
IO116NB3F10	AA24
IO116PB3F10	Y24
IO117NB3F10	AB25
IO117PB3F10	AA25
IO118NB3F11	T20
IO118PB3F11	R21
IO120NB3F11	W22
IO120PB3F11	W23
IO122NB3F11	V22
IO122PB3F11	U22
IO124NB3F11	Y23
IO124PB3F11	AA23
IO126NB3F11	V21
IO126PB3F11	U21
IO128NB3F11	Y22
IO128PB3F11	Y21
Bank 4	
IO129NB4F12	W20
IO129PB4F12	Y20

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO131NB4F12	V19
IO131PB4F12	W19
IO133NB4F12	Y18
IO133PB4F12	Y19
IO135NB4F12	W18
IO135PB4F12	V18
IO137NB4F12	Y17
IO137PB4F12	AA17
IO138NB4F12	AB19
IO138PB4F12	AB18
IO139NB4F13	AA19
IO139PB4F13	U18
IO140NB4F13	AC20
IO140PB4F13	AC21
IO141NB4F13	AD17
IO141PB4F13	AD18
IO142NB4F13	AD21
IO142PB4F13	AD22
IO143NB4F13	AB17
IO143PB4F13	AC17
IO144PB4F13	AE22
IO145NB4F13	AE15
IO145PB4F13	AE16
IO146NB4F13	AD19
IO146PB4F13	AD20
IO147NB4F13	AD15
IO147PB4F13	AD16
IO148PB4F13	AE21
IO149NB4F13	AD14
IO149PB4F13	AC14
IO150NB4F13	AE19
IO150PB4F13	AE20
IO151NB4F13	V17
IO151PB4F13	W17
IO152NB4F14	AB16
IO152PB4F14	W16

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO153NB4F14	Y15
IO153PB4F14	Y16
IO155NB4F14	V15
IO155PB4F14	V16
IO156NB4F14	AB14
IO156PB4F14	AB15
IO157NB4F14	AE14
IO157PB4F14	AC18
IO158NB4F14	AC15
IO158PB4F14	AC19
IO159NB4F14/CLKEN	W14
IO159PB4F14/CLKEP	W15
IO160NB4F14/CLKFN	AC13
IO160PB4F14/CLKFP	AD13
Bank 5	
IO161NB5F15/CLKGN	W13
IO161PB5F15/CLKGP	Y13
IO162NB5F15/CLKHN	AC12
IO162PB5F15/CLKHP	AD12
IO163NB5F15	V9
IO163PB5F15	V10
IO164NB5F15	V11
IO164PB5F15	T13
IO165NB5F15	U13
IO165PB5F15	V13
IO167NB5F15	W11
IO167PB5F15	W12
IO168NB5F15	AB6
IO168PB5F15	AA6
IO169NB5F15	V8
IO169PB5F15	V7
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	AB8
IO172PB5F16	AC8
IO173NB5F16	AA11

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO173PB5F16	Y11
IO174NB5F16	AB10
IO174PB5F16	AB11
IO175NB5F16	AC9
IO175PB5F16	AE9
IO177NB5F16	AA8
IO177PB5F16	Y8
IO178NB5F16	Y6
IO178PB5F16	W6
IO179NB5F16	Y10
IO179PB5F16	W10
IO180NB5F16	Y7
IO180PB5F16	W7
IO181NB5F17	AD9
IO181PB5F17	AD10
IO182NB5F17	AE10
IO182PB5F17	AE11
IO183NB5F17	AD7
IO183PB5F17	AD8
IO184NB5F17	AB9
IO185NB5F17	AE6
IO185PB5F17	AE7
IO186NB5F17	AE4
IO186PB5F17	AE5
IO187NB5F17	AA9
IO187PB5F17	Y9
IO188NB5F17	U8
IO189NB5F17	AD5
IO189PB5F17	AD6
IO191NB5F17	AC5
IO191PB5F17	AC6
IO192NB5F17	AB7
IO192PB5F17	AC7
Bank 6	
IO193NB6F18	U6
IO193PB6F18	U5

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO194NB6F18	Y3
IO194PB6F18	AA3
IO195NB6F18	V6
IO195PB6F18	W4
IO197NB6F18	R5
IO197PB6F18	U3
IO198NB6F18	P6
IO199NB6F18	Y5
IO199PB6F18	W5
IO200NB6F18	V3
IO200PB6F18	W3
IO201NB6F18	T7
IO201PB6F18	U7
IO202NB6F18	V2
IO203NB6F19	W2
IO203PB6F19	Y2
IO204NB6F19	AA1
IO204PB6F19	AB1
IO205NB6F19	R6
IO205PB6F19	T6
IO206NB6F19	W1
IO206PB6F19	Y1
IO207NB6F19	T2
IO207PB6F19	U2
IO208NB6F19	T1
IO208PB6F19	U1
IO209NB6F19	AA2
IO209PB6F19	AB2
IO210NB6F19	P5
IO211NB6F19	M1
IO211PB6F19	N1
IO212NB6F19	P1
IO212PB6F19	R1
IO213NB6F19	R8
IO213PB6F19	T8
IO215NB6F20	U4

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO215PB6F20	V4
IO216NB6F20	P8
IO216PB6F20	R3
IO217NB6F20	P7
IO217PB6F20	R7
IO219NB6F20	R4
IO219PB6F20	T4
IO220NB6F20	P2
IO220PB6F20	R2
IO221NB6F20	N4
IO221PB6F20	P4
IO223NB6F20	M2
IO223PB6F20	N2
IO224NB6F20	N3
IO224PB6F20	P3
Bank 7	
IO225NB7F21	J2
IO225PB7F21	J1
IO226PB7F21	G2
IO227NB7F21	H3
IO227PB7F21	H2
IO229NB7F21	K2
IO229PB7F21	L2
IO230NB7F21	K1
IO230PB7F21	L1
IO231NB7F21	E2
IO231PB7F21	F2
IO232NB7F21	F1
IO232PB7F21	G1
IO233NB7F21	L3
IO233PB7F21	M3
IO234NB7F21	D1
IO234PB7F21	E1
IO235NB7F21	K4
IO235PB7F21	L4
IO236NB7F22	M6

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
IO237NB7F22	N8
IO237PB7F22	N7
IO238NB7F22	M5
IO239NB7F22	L6
IO239PB7F22	L5
IO240NB7F22	M4
IO241NB7F22	L7
IO241PB7F22	M7
IO242NB7F22	J3
IO243NB7F22	M9
IO243PB7F22	M8
IO244NB7F22	P9
IO244PB7F22	N6
IO245NB7F22	K8
IO245PB7F22	L8
IO246NB7F22	F3
IO246PB7F22	E3
IO247NB7F23	K7
IO247PB7F23	K6
IO248NB7F23	D2
IO249NB7F23	G4
IO249PB7F23	G3
IO251NB7F23	N10
IO251PB7F23	N9
IO253NB7F23	H4
IO253PB7F23	J4
IO255NB7F23	J6
IO255PB7F23	J5
IO257NB7F23	H5
IO257PB7F23	H6
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
GND	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	T21
GND	T23
GND	T3
GND	T5

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
GND	V1
GND	V25
GND	V5
NC	A14
NC	AA12
NC	AA14
NC	AA20
NC	AB13
NC	AD4
NC	AE12
NC	E12
NC	E14
NC	F12
NC	F14
NC	F21
NC	G10
NC	H12
NC	H14
NC	J12
NC	J14
NC	U12
NC	U14
NC	V12
NC	V14
NC	Y12
NC	Y14
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5
TDI	C5
TDO	F6
TMS	D6
TRST	E6
V_{CCA}	AB20

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
V_{CCA}	F22
V_{CCA}	F4
V_{CCA}	J17
V_{CCA}	J9
V_{CCA}	K10
V_{CCA}	K11
V_{CCA}	K15
V_{CCA}	K16
V_{CCA}	L10
V_{CCA}	L16
V_{CCA}	R10
V_{CCA}	R16
V_{CCA}	T10
V_{CCA}	T11
V_{CCA}	T15
V_{CCA}	T16
V_{CCA}	U17
V_{CCA}	U9
V_{CCA}	Y4
V_{CCDA}	A12
V_{CCDA}	AA13
V_{CCDA}	AA15
V_{CCDA}	AA7
V_{CCDA}	AC11
V_{CCDA}	AD11
V_{CCDA}	AE17
V_{CCDA}	B15
V_{CCDA}	C15
V_{CCDA}	C6
V_{CCDA}	D13
V_{CCDA}	E13
V_{CCDA}	E19
V_{CCDA}	G5
V_{CCDA}	N21
V_{CCDA}	N5
V_{CCDA}	W21

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
$V_{CCI}B0$	A3
$V_{CCI}B0$	B3
$V_{CCI}B0$	C4
$V_{CCI}B0$	D5
$V_{CCI}B0$	J10
$V_{CCI}B0$	J11
$V_{CCI}B0$	K12
$V_{CCI}B1$	A23
$V_{CCI}B1$	B23
$V_{CCI}B1$	C22
$V_{CCI}B1$	D21
$V_{CCI}B1$	J15
$V_{CCI}B1$	J16
$V_{CCI}B1$	K14
$V_{CCI}B2$	C24
$V_{CCI}B2$	C25
$V_{CCI}B2$	D23
$V_{CCI}B2$	E22
$V_{CCI}B2$	K17
$V_{CCI}B2$	L17
$V_{CCI}B2$	M16
$V_{CCI}B3$	AA22
$V_{CCI}B3$	AB23
$V_{CCI}B3$	AC24
$V_{CCI}B3$	AC25
$V_{CCI}B3$	P16
$V_{CCI}B3$	R17
$V_{CCI}B3$	T17
$V_{CCI}B4$	AB21
$V_{CCI}B4$	AC22
$V_{CCI}B4$	AD23
$V_{CCI}B4$	AE23
$V_{CCI}B4$	T14
$V_{CCI}B4$	U15
$V_{CCI}B4$	U16
$V_{CCI}B5$	AB5

624-Pin CCGA/LGA	
RTAX1000S/SL Function	**Pin Number**
$V_{CCI}B5$	AC4
$V_{CCI}B5$	AD3
$V_{CCI}B5$	AE3
$V_{CCI}B5$	T12
$V_{CCI}B5$	U10
$V_{CCI}B5$	U11
$V_{CCI}B6$	AA4
$V_{CCI}B6$	AB3
$V_{CCI}B6$	AC1
$V_{CCI}B6$	AC2
$V_{CCI}B6$	P10
$V_{CCI}B6$	R9
$V_{CCI}B6$	T9
$V_{CCI}B7$	C1
$V_{CCI}B7$	C2
$V_{CCI}B7$	D3
$V_{CCI}B7$	E4
$V_{CCI}B7$	K9
$V_{CCI}B7$	L9
$V_{CCI}B7$	M10
V_{PUMP}	E20

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
Bank 0	
IO00NB0F0	D7
IO00PB0F0	E7
IO01NB0F0	G7
IO01PB0F0	G6
IO02NB0F0	B5
IO02PB0F0	B4
IO04PB0F0	C7
IO05NB0F0	F8
IO05PB0F0	F7
IO06NB0F0	H8
IO06PB0F0	H7
IO11NB0F0	J8
IO11PB0F0	J7
IO12PB0F1	B6
IO13NB0F1	E9
IO13PB0F1	D8
IO15NB0F1	C9
IO15PB0F1	C8
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	G9
IO19PB0F1	G8
IO20PB0F1	B7
IO23NB0F2	F10
IO23PB0F2	F9
IO26NB0F2	C11
IO26PB0F2	B8
IO27NB0F2	H10
IO27PB0F2	H9
IO28NB0F2	A9
IO28PB0F2	B9

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO30NB0F2	B11
IO30PB0F2	B10
IO31NB0F2	E11
IO31PB0F2	F11
IO33NB0F2	D12
IO33PB0F2	D11
IO34NB0F3	A11
IO34PB0F3	A10
IO37NB0F3	J13
IO37PB0F3	K13
IO38NB0F3	H11
IO38PB0F3	G11
IO40PB0F3	B12
IO41NB0F3/HCLKAN	G13
IO41PB0F3/HCLKAP	G12
IO42NB0F3/HCLKBN	C13
IO42PB0F3/HCLKBP	C12
Bank 1	
IO43NB1F4/HCLKCN	G15
IO43PB1F4/HCLKCP	G14
IO44NB1F4/HCLKDN	B14
IO44PB1F4/HCLKDP	B13
IO45NB1F4	H13
IO47NB1F4	D14
IO47PB1F4	C14
IO48NB1F4	A16
IO48PB1F4	A15
IO49PB1F4	H15
IO51NB1F4	E15
IO51PB1F4	F15
IO52NB1F4	A17
IO55NB1F5	G16
IO55PB1F5	H16
IO56NB1F5	A20
IO56PB1F5	A19
IO57NB1F5	D16

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO57PB1F5	D15
IO58NB1F5	A22
IO58PB1F5	A21
IO59NB1F5	F16
IO61NB1F5	G17
IO61PB1F5	H17
IO62NB1F5	B17
IO62PB1F5	B16
IO63NB1F5	H18
IO65NB1F6	C17
IO66PB1F6	B18
IO67NB1F6	J18
IO67PB1F6	J19
IO68NB1F6	B20
IO68PB1F6	B19
IO69NB1F6	E17
IO69PB1F6	F17
IO70NB1F6	B22
IO70PB1F6	B21
IO71PB1F6	G18
IO73NB1F6	G19
IO74NB1F6	C19
IO74PB1F6	C18
IO75NB1F6	D18
IO75PB1F6	D17
IO76NB1F7	C21
IO76PB1F7	C20
IO79NB1F7	H20
IO79PB1F7	H19
IO80NB1F7	E18
IO80PB1F7	F18
IO81NB1F7	G21
IO81PB1F7	G20
IO82NB1F7	F20
IO82PB1F7	F19
IO85NB1F7	D20

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO85PB1F7	D19
Bank 2	
IO86NB2F8	F23
IO86PB2F8	E23
IO87NB2F8	H23
IO87PB2F8	G23
IO88NB2F8	E24
IO88PB2F8	D24
IO89NB2F8	M17
IO89PB2F8	G22
IO91NB2F8	J22
IO91PB2F8	H22
IO92NB2F8	L18
IO92PB2F8	K18
IO96NB2F9	G24
IO96PB2F9	F24
IO97NB2F9	J21
IO97PB2F9	J20
IO98PB2F9	J23
IO99NB2F9	L19
IO99PB2F9	K19
IO100NB2F9	E25
IO100PB2F9	D25
IO103PB2F9	K20
IO105NB2F9	M19
IO105PB2F9	M18
IO106NB2F9	J24
IO106PB2F9	H24
IO107NB2F10	L23
IO107PB2F10	N16
IO109NB2F10	L22
IO109PB2F10	K22
IO110NB2F10	G25
IO110PB2F10	F25
IO111NB2F10	L21
IO111PB2F10	L20

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO112NB2F10	L24
IO112PB2F10	K24
IO113NB2F10	N17
IO115NB2F10	M20
IO115PB2F10	M21
IO117NB2F10	N19
IO117PB2F10	N18
IO118NB2F11	J25
IO121NB2F11	N24
IO121PB2F11	M24
IO122NB2F11	L25
IO122PB2F11	K25
IO123NB2F11	N22
IO123PB2F11	M22
IO124NB2F11	N23
IO124PB2F11	M23
IO127NB2F11	P18
IO127PB2F11	P17
IO128NB2F11	N25
IO128PB2F11	M25
Bank 3	
IO129NB3F12	N20
IO130PB3F12	P24
IO131NB3F12	P21
IO133NB3F12	P20
IO133PB3F12	P19
IO138NB3F12	R23
IO138PB3F12	P23
IO139NB3F13	R22
IO139PB3F13	P22
IO141NB3F13	R19
IO142NB3F13	R25
IO142PB3F13	P25
IO143PB3F13	R21
IO145NB3F13	T18
IO145PB3F13	R18

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO146NB3F13	T24
IO146PB3F13	R24
IO147NB3F13	T20
IO147PB3F13	R20
IO148NB3F13	U25
IO148PB3F13	T25
IO149NB3F13	T22
IO153NB3F14	U19
IO153PB3F14	T19
IO154NB3F14	Y25
IO154PB3F14	W25
IO157NB3F14	V20
IO157PB3F14	U20
IO158NB3F14	AB25
IO158PB3F14	AA25
IO160PB3F14	W24
IO161NB3F15	U24
IO161PB3F15	U23
IO162NB3F15	AA24
IO162PB3F15	Y24
IO163NB3F15	V22
IO163PB3F15	U22
IO164NB3F15	V23
IO164PB3F15	V24
IO166NB3F15	AB24
IO167NB3F15	V21
IO167PB3F15	U21
IO168NB3F15	Y23
IO168PB3F15	AA23
IO169NB3F15	W22
IO169PB3F15	W23
IO170NB3F15	Y22
IO170PB3F15	Y21
Bank 4	
IO171NB4F16	AC20
IO171PB4F16	AC21

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO172NB4F16	W20
IO172PB4F16	Y20
IO173NB4F16	AD21
IO173PB4F16	AD22
IO174NB4F16	AA19
IO176NB4F16	Y18
IO176PB4F16	Y19
IO177NB4F16	AB19
IO177PB4F16	AB18
IO182NB4F17	V19
IO182PB4F17	W19
IO183PB4F17	AC19
IO184NB4F17	AB17
IO184PB4F17	AC17
IO185NB4F17	AD19
IO185PB4F17	AD20
IO187PB4F17	AC18
IO188NB4F17	Y17
IO188PB4F17	AA17
IO189PB4F17	AE22
IO191NB4F17	W18
IO191PB4F17	V18
IO192PB4F17	U18
IO195PB4F18	AE21
IO196NB4F18	AB16
IO197NB4F18	AD17
IO197PB4F18	AD18
IO198NB4F18	V17
IO198PB4F18	W17
IO199NB4F18	AE19
IO199PB4F18	AE20
IO200NB4F18	AC15
IO201NB4F18	AD15
IO201PB4F18	AD16
IO202NB4F18	Y15
IO202PB4F18	Y16

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO206NB4F19	AB14
IO206PB4F19	AB15
IO207NB4F19	AE15
IO207PB4F19	AE16
IO208PB4F19	W16
IO209NB4F19	AE14
IO210NB4F19	V15
IO210PB4F19	V16
IO211NB4F19	AD14
IO211PB4F19	AC14
IO212NB4F19/CLKEN	W14
IO212PB4F19/CLKEP	W15
IO213NB4F19/CLKFN	AC13
IO213PB4F19/CLKFP	AD13
Bank 5	
IO214NB5F20/CLKGN	W13
IO214PB5F20/CLKGP	Y13
IO215NB5F20/CLKHN	AC12
IO215PB5F20/CLKHP	AD12
IO216NB5F20	U13
IO216PB5F20	V13
IO217NB5F20	AE10
IO217PB5F20	AE11
IO218NB5F20	W11
IO218PB5F20	W12
IO222NB5F20	AA11
IO222PB5F20	Y11
IO223PB5F21	AE9
IO225NB5F21	AE6
IO225PB5F21	AE7
IO226NB5F21	Y10
IO226PB5F21	W10
IO227PB5F21	T13
IO228NB5F21	AB10
IO228PB5F21	AB11
IO229NB5F21	AD9

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO229PB5F21	AD10
IO230NB5F21	V11
IO233NB5F21	AD7
IO233PB5F21	AD8
IO234NB5F21	V9
IO234PB5F21	V10
IO236NB5F22	AC9
IO238NB5F22	W8
IO238PB5F22	W9
IO239NB5F22	AE4
IO239PB5F22	AE5
IO240NB5F22	AB9
IO242NB5F22	AA9
IO242PB5F22	Y9
IO243NB5F22	AD5
IO243PB5F22	AD6
IO244NB5F22	U8
IO246NB5F23	AB8
IO246PB5F23	AC8
IO247NB5F23	AB7
IO247PB5F23	AC7
IO250NB5F23	AA8
IO250PB5F23	Y8
IO251NB5F23	V8
IO251PB5F23	V7
IO252NB5F23	Y7
IO252PB5F23	W7
IO253NB5F23	AC5
IO253PB5F23	AC6
IO254NB5F23	Y6
IO254PB5F23	W6
IO256NB5F23	AB6
IO256PB5F23	AA6
Bank 6	
IO257NB6F24	Y3
IO257PB6F24	AA3

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO258NB6F24	V3
IO258PB6F24	W3
IO259NB6F24	AA2
IO259PB6F24	AB2
IO260NB6F24	V6
IO260PB6F24	W4
IO262NB6F24	U4
IO262PB6F24	V4
IO263NB6F24	Y5
IO263PB6F24	W5
IO268NB6F25	U6
IO268PB6F25	U5
IO269PB6F25	U3
IO272NB6F25	T2
IO272PB6F25	U2
IO273NB6F25	W2
IO273PB6F25	Y2
IO274NB6F25	R6
IO274PB6F25	T6
IO275NB6F25	T7
IO275PB6F25	U7
IO277NB6F25	V2
IO278NB6F26	R4
IO278PB6F26	T4
IO279PB6F26	R3
IO280NB6F26	R5
IO281NB6F26	AA1
IO281PB6F26	AB1
IO284NB6F26	R8
IO284PB6F26	T8
IO285NB6F26	W1
IO285PB6F26	Y1
IO286NB6F26	P2
IO286PB6F26	R2
IO287NB6F26	T1
IO287PB6F26	U1

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO288NB6F26	P5
IO290NB6F27	P6
IO291NB6F27	P1
IO291PB6F27	R1
IO292NB6F27	P7
IO292PB6F27	R7
IO293NB6F27	M1
IO293PB6F27	N1
IO294NB6F27	P8
IO296NB6F27	N3
IO296PB6F27	P3
IO298NB6F27	N4
IO298PB6F27	P4
IO299NB6F27	M2
IO299PB6F27	N2
Bank 7	
IO300NB7F28	P9
IO300PB7F28	N6
IO302NB7F28	M6
IO304NB7F28	N8
IO304PB7F28	N7
IO308NB7F28	M4
IO309NB7F28	L3
IO309PB7F28	M3
IO310NB7F29	N10
IO310PB7F29	N9
IO311NB7F29	K1
IO311PB7F29	L1
IO313NB7F29	M5
IO316NB7F29	L6
IO316PB7F29	L5
IO317NB7F29	K2
IO317PB7F29	L2
IO318NB7F29	K4
IO318PB7F29	L4
IO320NB7F29	J3

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO321NB7F30	J2
IO321PB7F30	J1
IO323NB7F30	L7
IO323PB7F30	M7
IO324NB7F30	M9
IO324PB7F30	M8
IO327NB7F30	F1
IO327PB7F30	G1
IO328NB7F30	K7
IO328PB7F30	K6
IO329NB7F30	D1
IO329PB7F30	E1
IO331PB7F30	G2
IO332NB7F31	H3
IO332PB7F31	H2
IO333NB7F31	E2
IO333PB7F31	F2
IO334NB7F31	H4
IO334PB7F31	J4
IO335NB7F31	H5
IO335PB7F31	H6
IO337NB7F31	D2
IO338NB7F31	J6
IO338PB7F31	J5
IO339NB7F31	F3
IO339PB7F31	E3
IO340NB7F31	G4
IO340PB7F31	G3
IO341NB7F31	K8
IO341PB7F31	L8
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	T21
GND	T23
GND	T3
GND	T5

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	V1
GND	V25
GND	V5
NC	AA12
NC	AA14
NC	E12
NC	E14
NC	F12
NC	F14
NC	H12
NC	H14
NC	J12
NC	J14
NC	U12
NC	U14
NC	V12
NC	V14
NC	Y12
NC	Y14
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5
TDI	C5
TDO	F6
TMS	D6
TRST	E6
V_{CCA}	AB20
V_{CCA}	F22
V_{CCA}	F4
V_{CCA}	J17
V_{CCA}	J9
V_{CCA}	K10
V_{CCA}	K11
V_{CCA}	K15

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
V_{CCA}	K16
V_{CCA}	L10
V_{CCA}	L16
V_{CCA}	R10
V_{CCA}	R16
V_{CCA}	T10
V_{CCA}	T11
V_{CCA}	T15
V_{CCA}	T16
V_{CCA}	U17
V_{CCA}	U9
V_{CCA}	Y4
V_{CCDA}	A12
V_{CCDA}	A14
V_{CCDA}	AA13
V_{CCDA}	AA15
V_{CCDA}	AA20
V_{CCDA}	AA7
V_{CCDA}	AB13
V_{CCDA}	AC11
V_{CCDA}	AD11
V_{CCDA}	AD4
V_{CCDA}	AE12
V_{CCDA}	AE17
V_{CCDA}	B15
V_{CCDA}	C15
V_{CCDA}	C6
V_{CCDA}	D13
V_{CCDA}	E13
V_{CCDA}	E19
V_{CCDA}	F21
V_{CCDA}	G10
V_{CCDA}	G5
V_{CCDA}	N21
V_{CCDA}	N5
V_{CCDA}	W21

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B0$	A3
$V_{CCI}B0$	B3
$V_{CCI}B0$	C4
$V_{CCI}B0$	D5
$V_{CCI}B0$	J10
$V_{CCI}B0$	J11
$V_{CCI}B0$	K12
$V_{CCI}B1$	A23
$V_{CCI}B1$	B23
$V_{CCI}B1$	C22
$V_{CCI}B1$	D21
$V_{CCI}B1$	J15
$V_{CCI}B1$	J16
$V_{CCI}B1$	K14
$V_{CCI}B2$	C24
$V_{CCI}B2$	C25
$V_{CCI}B2$	D23
$V_{CCI}B2$	E22
$V_{CCI}B2$	K17
$V_{CCI}B2$	L17
$V_{CCI}B2$	M16
$V_{CCI}B3$	AA22
$V_{CCI}B3$	AB23
$V_{CCI}B3$	AC24
$V_{CCI}B3$	AC25
$V_{CCI}B3$	P16
$V_{CCI}B3$	R17
$V_{CCI}B3$	T17
$V_{CCI}B4$	AB21
$V_{CCI}B4$	AC22
$V_{CCI}B4$	AD23
$V_{CCI}B4$	AE23
$V_{CCI}B4$	T14
$V_{CCI}B4$	U15
$V_{CCI}B4$	U16
$V_{CCI}B5$	AB5

624-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B5$	AC4
$V_{CCI}B5$	AD3
$V_{CCI}B5$	AE3
$V_{CCI}B5$	T12
$V_{CCI}B5$	U10
$V_{CCI}B5$	U11
$V_{CCI}B6$	AA4
$V_{CCI}B6$	AB3
$V_{CCI}B6$	AC1
$V_{CCI}B6$	AC2
$V_{CCI}B6$	P10
$V_{CCI}B6$	R9
$V_{CCI}B6$	T9
$V_{CCI}B7$	C1
$V_{CCI}B7$	C2
$V_{CCI}B7$	D3
$V_{CCI}B7$	E4
$V_{CCI}B7$	K9
$V_{CCI}B7$	L9
$V_{CCI}B7$	M10
V_{PUMP}	E20

1152-Pin CCGA/LGA

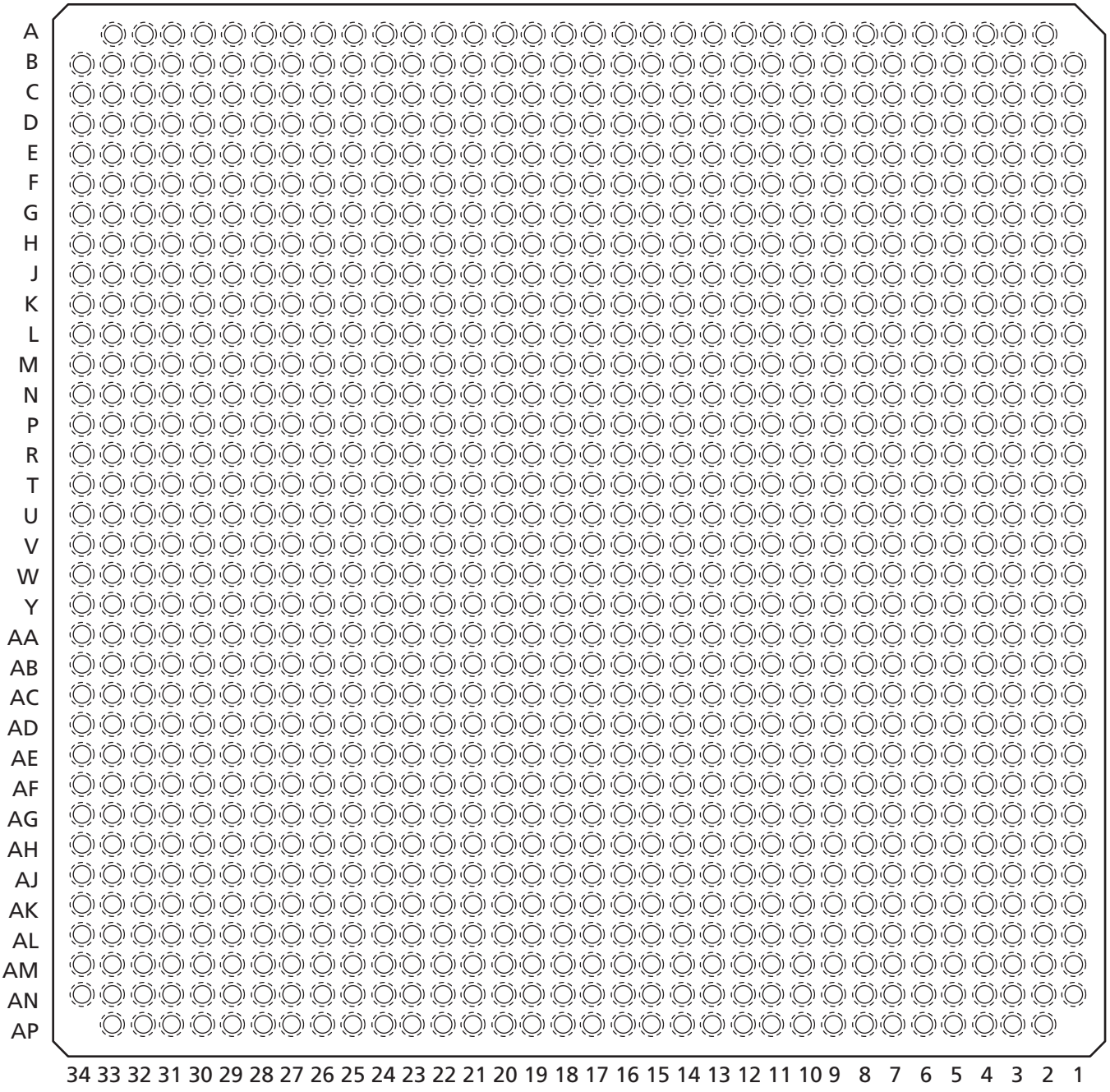


Figure 3-5 • **1152-Pin CCGA/LGA (Bottom View)**

Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
Bank 0	
IO00NB0F0	D6
IO00PB0F0	C6
IO01NB0F0	H10
IO01PB0F0	H9
IO02NB0F0	F8
IO02PB0F0	G8
IO03NB0F0	A6
IO03PB0F0	B6
IO04NB0F0	C7
IO04PB0F0	D7
IO05NB0F0	K10
IO05PB0F0	J10
IO06NB0F0	F9
IO06PB0F0	G9
IO07NB0F0	F10
IO07PB0F0	G10
IO08NB0F0	E9
IO08PB0F0	E8
IO09NB0F0	J11
IO09PB0F0	K11
IO10NB0F0	C8
IO10PB0F0	D8
IO11NB0F0	K12
IO11PB0F0	J12
IO12NB0F1	G11
IO12PB0F1	H11
IO13NB0F1	G12
IO13PB0F1	H12
IO14NB0F1	A7
IO14PB0F1	B7
IO15NB0F1	H13
IO15PB0F1	J13
IO16NB0F1	C9
IO16PB0F1	D9
IO17NB0F1	F12
IO17PB0F1	F11

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO18NB0F1	E11
IO18PB0F1	E10
IO19NB0F1	F13
IO19PB0F1	G13
IO20NB0F1	A10
IO20PB0F1	A9
IO21NB0F1	K14
IO21PB0F1	K13
IO22NB0F2	B11
IO22PB0F2	B10
IO23NB0F2	C12
IO23PB0F2	C11
IO24NB0F2	A12
IO24PB0F2	A11
IO25NB0F2	H14
IO25PB0F2	J14
IO26NB0F2	D13
IO26PB0F2	D12
IO27NB0F2	F14
IO27PB0F2	G14
IO28NB0F2	E14
IO28PB0F2	E13
IO29NB0F2	B13
IO29PB0F2	B12
IO30NB0F2	C14
IO30PB0F2	C13
IO31NB0F2	H15
IO31PB0F2	J15
IO32NB0F2	A14
IO32PB0F2	B14
IO33NB0F2	K15
IO33PB0F2	L15
IO34NB0F3	D15
IO34PB0F3	D14
IO35NB0F3	A15
IO35PB0F3	B15
IO36NB0F3	B16

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO36PB0F3	A16
IO37NB0F3	G16
IO37PB0F3	G15
IO38NB0F3	D16
IO38PB0F3	C16
IO39NB0F3	K16
IO39PB0F3	L16
IO40NB0F3	D17
IO40PB0F3	C17
IO41NB0F3/HCLKAN	E16
IO41PB0F3/HCLKAP	F16
IO42NB0F3/HCLKBN	G17
IO42PB0F3/HCLKBP	F17
Bank 1	
IO43NB1F4/HCLKCN	G19
IO43PB1F4/HCLKCP	G18
IO44NB1F4/HCLKDN	E19
IO44PB1F4/HCLKDP	F19
IO45NB1F4	C18
IO45PB1F4	D18
IO46NB1F4	A18
IO46PB1F4	B18
IO47NB1F4	K19
IO47PB1F4	L19
IO48NB1F4	C19
IO48PB1F4	D19
IO49NB1F4	K20
IO49PB1F4	L20
IO50NB1F4	A19
IO50PB1F4	B19
IO51NB1F4	H20
IO51PB1F4	J20
IO52NB1F4	B20
IO52PB1F4	A20
IO53NB1F4	F20
IO53PB1F4	E20
IO54NB1F5	B21

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO54PB1F5	A21
IO55NB1F5	K21
IO55PB1F5	J21
IO56NB1F5	D21
IO56PB1F5	C21
IO57NB1F5	G22
IO57PB1F5	G21
IO58NB1F5	E22
IO58PB1F5	E21
IO59NB1F5	D22
IO59PB1F5	C22
IO60NB1F5	B23
IO60PB1F5	A23
IO61NB1F5	H22
IO61PB1F5	H21
IO62NB1F5	C24
IO62PB1F5	C23
IO63NB1F5	F23
IO63PB1F5	F22
IO64NB1F6	B24
IO64PB1F6	A24
IO65NB1F6	J22
IO65PB1F6	K22
IO66NB1F6	B25
IO66PB1F6	A25
IO67NB1F6	K23
IO67PB1F6	J23
IO68NB1F6	F24
IO68PB1F6	E24
IO69NB1F6	C27
IO69PB1F6	C26
IO70NB1F6	H24
IO70PB1F6	G24
IO71NB1F6	H23
IO71PB1F6	G23
IO72NB1F6	B28
IO72PB1F6	A28

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO73NB1F6	E26
IO73PB1F6	E25
IO74NB1F6	F26
IO74PB1F6	F25
IO75NB1F6	K25
IO75PB1F6	K24
IO76NB1F7	D27
IO76PB1F7	D26
IO77NB1F7	B29
IO77PB1F7	A29
IO78NB1F7	D28
IO78PB1F7	C28
IO79NB1F7	H25
IO79PB1F7	G25
IO80NB1F7	F27
IO80PB1F7	E27
IO81NB1F7	J25
IO81PB1F7	J24
IO82NB1F7	D29
IO82PB1F7	C29
IO83NB1F7	H26
IO83PB1F7	G26
IO84NB1F7	F28
IO84PB1F7	E28
IO85NB1F7	H27
IO85PB1F7	G27
Bank 2	
IO86NB2F8	J28
IO86PB2F8	J27
IO87NB2F8	M25
IO87PB2F8	L25
IO88NB2F8	L26
IO88PB2F8	K26
IO89NB2F8	G31
IO89PB2F8	F31
IO90NB2F8	H29
IO90PB2F8	G29

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO91NB2F8	K28
IO91PB2F8	K27
IO92NB2F8	J30
IO92PB2F8	H30
IO93NB2F8	L28
IO93PB2F8	L27
IO94NB2F8	K29
IO94PB2F8	J29
IO95NB2F8	K31
IO95PB2F8	J31
IO96NB2F9	J32
IO96PB2F9	H32
IO97NB2F9	M27
IO97PB2F9	M26
IO98NB2F9	L30
IO98PB2F9	K30
IO99NB2F9	N25
IO99PB2F9	N26
IO100NB2F9	M29
IO100PB2F9	L29
IO101NB2F9	L33
IO101PB2F9	L32
IO102NB2F9	K34
IO102PB2F9	K33
IO103NB2F9	N28
IO103PB2F9	M28
IO104NB2F9	M34
IO104PB2F9	L34
IO105NB2F9	P27
IO105PB2F9	N27
IO106NB2F9	M32
IO106PB2F9	M31
IO107NB2F10	P25
IO107PB2F10	P26
IO108NB2F10	N33
IO108PB2F10	M33
IO109NB2F10	P29

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO109PB2F10	N29
IO110NB2F10	P30
IO110PB2F10	N30
IO111NB2F10	R24
IO111PB2F10	R25
IO112NB2F10	P31
IO112PB2F10	N31
IO113NB2F10	R28
IO113PB2F10	P28
IO114NB2F10	P32
IO114PB2F10	N32
IO115NB2F10	R30
IO115PB2F10	R29
IO116NB2F10	P34
IO116PB2F10	P33
IO117NB2F10	R27
IO117PB2F10	R26
IO118NB2F11	R34
IO118PB2F11	R33
IO119NB2F11	T24
IO119PB2F11	T25
IO120NB2F11	T33
IO120PB2F11	T34
IO121NB2F11	T27
IO121PB2F11	T26
IO122NB2F11	T30
IO122PB2F11	T29
IO123NB2F11	U28
IO123PB2F11	T28
IO124NB2F11	T31
IO124PB2F11	T32
IO125NB2F11	U24
IO125PB2F11	U25
IO126NB2F11	U33
IO126PB2F11	U34
IO127NB2F11	U26
IO127PB2F11	U27

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO128NB2F11	U31
IO128PB2F11	U32
Bank 3	
IO129NB3F12	V29
IO129PB3F12	U29
IO130NB3F12	V31
IO130PB3F12	V32
IO131NB3F12	V24
IO131PB3F12	V25
IO132NB3F12	W28
IO132PB3F12	V28
IO133NB3F12	W26
IO133PB3F12	V26
IO134NB3F12	W33
IO134PB3F12	V33
IO135NB3F12	W25
IO135PB3F12	W24
IO136NB3F12	W31
IO136PB3F12	W32
IO137NB3F12	Y30
IO137PB3F12	W30
IO138NB3F12	Y29
IO138PB3F12	W29
IO139NB3F13	Y27
IO139PB3F13	W27
IO140NB3F13	AA33
IO140PB3F13	Y33
IO141NB3F13	Y25
IO141PB3F13	Y24
IO142NB3F13	AA31
IO142PB3F13	Y31
IO143NB3F13	AA28
IO143PB3F13	Y28
IO144NB3F13	AA34
IO144PB3F13	Y34
IO145NB3F13	AA26
IO145PB3F13	Y26

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO146NB3F13	AA29
IO146PB3F13	AA30
IO147NB3F13	AB30
IO147PB3F13	AB29
IO148NB3F13	AB32
IO148PB3F13	AA32
IO149NB3F13	AB27
IO149PB3F13	AA27
IO150NB3F14	AC31
IO150PB3F14	AB31
IO151NB3F14	AD33
IO151PB3F14	AC33
IO152NB3F14	AC28
IO152PB3F14	AB28
IO153NB3F14	AB25
IO153PB3F14	AA25
IO154NB3F14	AD32
IO154PB3F14	AC32
IO155NB3F14	AD29
IO155PB3F14	AC29
IO156NB3F14	AE30
IO156PB3F14	AD30
IO157NB3F14	AC26
IO157PB3F14	AB26
IO158NB3F14	AH33
IO158PB3F14	AG33
IO159NB3F14	AD27
IO159PB3F14	AC27
IO160NB3F14	AG32
IO160PB3F14	AF32
IO161NB3F15	AG31
IO161PB3F15	AF31
IO162NB3F15	AF29
IO162PB3F15	AE29
IO163NB3F15	AE28
IO163PB3F15	AD28
IO164NB3F15	AG30

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO164PB3F15	AF30
IO165NB3F15	AE26
IO165PB3F15	AD26
IO166NB3F15	AJ30
IO166PB3F15	AH30
IO167NB3F15	AG28
IO167PB3F15	AF28
IO168NB3F15	AF27
IO168PB3F15	AE27
IO169NB3F15	AH29
IO169PB3F15	AG29
IO170NB3F15	AD25
IO170PB3F15	AC25
Bank 4	
IO171NB4F16	AP29
IO171PB4F16	AN29
IO172NB4F16	AH26
IO172PB4F16	AH27
IO173NB4F16	AJ27
IO173PB4F16	AJ28
IO174NB4F16	AL27
IO174PB4F16	AL28
IO175NB4F16	AM28
IO175PB4F16	AM29
IO176NB4F16	AG25
IO176PB4F16	AG26
IO177NB4F16	AK26
IO177PB4F16	AK27
IO178NB4F16	AF25
IO178PB4F16	AE25
IO179NB4F16	AP28
IO179PB4F16	AN28
IO180NB4F16	AJ25
IO180PB4F16	AJ26
IO181NB4F17	AM26
IO181PB4F17	AM27
IO182NB4F17	AF24

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO182PB4F17	AE24
IO183NB4F17	AH24
IO183PB4F17	AH25
IO184NB4F17	AG23
IO184PB4F17	AG24
IO185NB4F17	AL25
IO185PB4F17	AL26
IO186NB4F17	AP25
IO186PB4F17	AP26
IO187NB4F17	AK24
IO187PB4F17	AK25
IO188NB4F17	AF23
IO188PB4F17	AE23
IO189NB4F17	AN24
IO189PB4F17	AM24
IO190NB4F17	AH22
IO190PB4F17	AH23
IO191NB4F17	AJ23
IO191PB4F17	AJ24
IO192NB4F17	AG21
IO192PB4F17	AG22
IO193NB4F18	AP23
IO193PB4F18	AP24
IO194NB4F18	AN22
IO194PB4F18	AN23
IO195NB4F18	AM23
IO195PB4F18	AL23
IO196NB4F18	AF21
IO196PB4F18	AF22
IO197NB4F18	AL22
IO197PB4F18	AM22
IO198NB4F18	AE21
IO198PB4F18	AE22
IO199NB4F18	AJ21
IO199PB4F18	AJ22
IO200NB4F18	AK21
IO200PB4F18	AK22

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO201NB4F18	AM21
IO201PB4F18	AL21
IO202NB4F18	AE20
IO202PB4F18	AD20
IO203NB4F19	AN21
IO203PB4F19	AP21
IO204NB4F19	AP20
IO204PB4F19	AN20
IO205NB4F19	AN19
IO205PB4F19	AP19
IO206NB4F19	AG20
IO206PB4F19	AF20
IO207NB4F19	AL19
IO207PB4F19	AL20
IO208NB4F19	AG19
IO208PB4F19	AF19
IO209NB4F19	AN18
IO209PB4F19	AP18
IO210NB4F19	AE19
IO210PB4F19	AD19
IO211NB4F19	AL18
IO211PB4F19	AM18
IO212NB4F19/CLKEN	AJ20
IO212PB4F19/CLKEP	AK20
IO213NB4F19/CLKFN	AJ18
IO213PB4F19/CLKFP	AJ19
Bank 5	
IO214NB5F20/CLKGN	AJ16
IO214PB5F20/CLKGP	AJ17
IO215NB5F20/CLKHN	AJ15
IO215PB5F20/CLKHP	AK15
IO216NB5F20	AD16
IO216PB5F20	AE17
IO217NB5F20	AM17
IO217PB5F20	AL17
IO218NB5F20	AG16
IO218PB5F20	AF16

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO219NB5F20	AM16
IO219PB5F20	AL16
IO220NB5F20	AP16
IO220PB5F20	AN16
IO221NB5F20	AN15
IO221PB5F20	AP15
IO222NB5F20	AD15
IO222PB5F20	AE16
IO223NB5F21	AL14
IO223PB5F21	AL15
IO224NB5F21	AN14
IO224PB5F21	AP14
IO225NB5F21	AK13
IO225PB5F21	AK14
IO226NB5F21	AE15
IO226PB5F21	AF15
IO227NB5F21	AG14
IO227PB5F21	AG15
IO228NB5F21	AJ13
IO228PB5F21	AJ14
IO229NB5F21	AM13
IO229PB5F21	AM14
IO230NB5F21	AE14
IO230PB5F21	AF14
IO231NB5F21	AN12
IO231PB5F21	AP12
IO232NB5F21	AG13
IO232PB5F21	AH13
IO233NB5F21	AL12
IO233PB5F21	AL13
IO234NB5F21	AE13
IO234PB5F21	AF13
IO235NB5F22	AN11
IO235PB5F22	AP11
IO236NB5F22	AM11
IO236PB5F22	AM12
IO237NB5F22	AJ11

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO237PB5F22	AJ12
IO238NB5F22	AH11
IO238PB5F22	AH12
IO239NB5F22	AK10
IO239PB5F22	AK11
IO240NB5F22	AE12
IO240PB5F22	AF12
IO241NB5F22	AN10
IO241PB5F22	AP10
IO242NB5F22	AG11
IO242PB5F22	AG12
IO243NB5F22	AL9
IO243PB5F22	AL10
IO244NB5F22	AM8
IO244PB5F22	AM9
IO245NB5F23	AH10
IO245PB5F23	AJ10
IO246NB5F23	AF10
IO246PB5F23	AF11
IO247NB5F23	AJ9
IO247PB5F23	AK9
IO248NB5F23	AN7
IO248PB5F23	AP7
IO249NB5F23	AL7
IO249PB5F23	AL8
IO250NB5F23	AE10
IO250PB5F23	AE11
IO251NB5F23	AK8
IO251PB5F23	AJ8
IO252NB5F23	AH8
IO252PB5F23	AH9
IO253NB5F23	AN6
IO253PB5F23	AP6
IO254NB5F23	AG9
IO254PB5F23	AG10
IO255NB5F23	AJ7
IO255PB5F23	AK7

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO256NB5F23	AL6
IO256PB5F23	AM6
Bank 6	
IO257NB6F24	AG6
IO257PB6F24	AH6
IO258NB6F24	AD9
IO258PB6F24	AE9
IO259NB6F24	AF7
IO259PB6F24	AG7
IO260NB6F24	AH3
IO260PB6F24	AH4
IO261NB6F24	AH5
IO261PB6F24	AJ5
IO262NB6F24	AE6
IO262PB6F24	AF6
IO263NB6F24	AF5
IO263PB6F24	AG5
IO264NB6F24	AD8
IO264PB6F24	AE8
IO265NB6F24	AF3
IO265PB6F24	AG3
IO266NB6F24	AC10
IO266PB6F24	AD10
IO267NB6F25	AD7
IO267PB6F25	AE7
IO268NB6F25	AD5
IO268PB6F25	AE5
IO269NB6F25	AE4
IO269PB6F25	AF4
IO270NB6F25	AB9
IO270PB6F25	AC9
IO271NB6F25	AC6
IO271PB6F25	AD6
IO272NB6F25	AB8
IO272PB6F25	AC8
IO273NB6F25	AE1
IO273PB6F25	AE2

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO274NB6F25	AA10
IO274PB6F25	AB10
IO275NB6F25	AB7
IO275PB6F25	AC7
IO276NB6F25	AD1
IO276PB6F25	AD2
IO277NB6F25	AC4
IO277PB6F25	AC3
IO278NB6F26	AA8
IO278PB6F26	AA9
IO279NB6F26	AB5
IO279PB6F26	AB6
IO280NB6F26	Y10
IO280PB6F26	Y11
IO281NB6F26	AB3
IO281PB6F26	AB4
IO282NB6F26	Y7
IO282PB6F26	AA7
IO283NB6F26	AC2
IO283PB6F26	AC1
IO284NB6F26	Y9
IO284PB6F26	Y8
IO285NB6F26	AA5
IO285PB6F26	AA6
IO286NB6F26	W10
IO286PB6F26	W11
IO287NB6F26	AA3
IO287PB6F26	AA4
IO288NB6F26	W9
IO288PB6F26	W8
IO289NB6F27	AA1
IO289PB6F27	AA2
IO290NB6F27	W6
IO290PB6F27	Y6
IO291NB6F27	W5
IO291PB6F27	Y5
IO292NB6F27	V7

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO292PB6F27	W7
IO293NB6F27	W4
IO293PB6F27	Y4
IO294NB6F27	V10
IO294PB6F27	V11
IO295NB6F27	Y1
IO295PB6F27	Y2
IO296NB6F27	W1
IO296PB6F27	W2
IO297NB6F27	V1
IO297PB6F27	V2
IO298NB6F27	V9
IO298PB6F27	V8
IO299NB6F27	U4
IO299PB6F27	V4
Bank 7	
IO300NB7F28	U10
IO300PB7F28	U11
IO301NB7F28	U2
IO301PB7F28	U1
IO302NB7F28	U6
IO302PB7F28	U7
IO303NB7F28	T3
IO303PB7F28	U3
IO304NB7F28	U9
IO304PB7F28	U8
IO305NB7F28	R2
IO305PB7F28	R1
IO306NB7F28	R4
IO306PB7F28	T4
IO307NB7F28	R5
IO307PB7F28	T5
IO308NB7F28	T11
IO308PB7F28	T10
IO309NB7F28	T6
IO309PB7F28	T7
IO310NB7F29	T9

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO310PB7F29	T8
IO311NB7F29	N3
IO311PB7F29	P3
IO312NB7F29	P7
IO312PB7F29	R7
IO313NB7F29	P6
IO313PB7F29	R6
IO314NB7F29	M2
IO314PB7F29	N2
IO315NB7F29	N4
IO315PB7F29	P4
IO316NB7F29	R9
IO316PB7F29	R8
IO317NB7F29	N5
IO317PB7F29	P5
IO318NB7F29	R10
IO318PB7F29	R11
IO319NB7F29	L2
IO319PB7F29	L1
IO320NB7F29	N8
IO320PB7F29	P8
IO321NB7F30	M6
IO321PB7F30	N6
IO322NB7F30	P10
IO322PB7F30	P9
IO323NB7F30	L3
IO323PB7F30	M3
IO324NB7F30	M7
IO324PB7F30	N7
IO325NB7F30	K2
IO325PB7F30	K1
IO326NB7F30	G2
IO326PB7F30	H2
IO327NB7F30	L6
IO327PB7F30	L5
IO328NB7F30	N10
IO328PB7F30	N9

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
IO329NB7F30	J4
IO329PB7F30	K4
IO330NB7F30	J5
IO330PB7F30	K5
IO331NB7F30	M10
IO331PB7F30	M9
IO332NB7F31	L8
IO332PB7F31	M8
IO333NB7F31	F2
IO333PB7F31	F1
IO334NB7F31	J6
IO334PB7F31	K6
IO335NB7F31	H4
IO335PB7F31	H3
IO336NB7F31	K7
IO336PB7F31	L7
IO337NB7F31	G4
IO337PB7F31	G3
IO338NB7F31	K9
IO338PB7F31	L9
IO339NB7F31	H6
IO339PB7F31	H5
IO340NB7F31	H7
IO340PB7F31	J7
IO341NB7F31	J8
IO341PB7F31	K8
Dedicated I/O	
GND	A13
GND	A2
GND	A22
GND	A27
GND	A3
GND	A31
GND	A32
GND	A33
GND	A4
GND	A8

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	AA14
GND	AA15
GND	AA16
GND	AA17
GND	AA18
GND	AA19
GND	AA20
GND	AA21
GND	AB1
GND	AB13
GND	AB22
GND	AB34
GND	AC12
GND	AC23
GND	AC30
GND	AC5
GND	AD11
GND	AD24
GND	AD31
GND	AD4
GND	AE3
GND	AE32
GND	AF2
GND	AF33
GND	AG1
GND	AG27
GND	AG34
GND	AG8
GND	AH28
GND	AH7
GND	AJ29
GND	AJ6
GND	AK12
GND	AK17
GND	AK18
GND	AK23
GND	AK30

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	AK5
GND	AL1
GND	AL11
GND	AL2
GND	AL24
GND	AL3
GND	AL31
GND	AL32
GND	AL33
GND	AL34
GND	AL4
GND	AM1
GND	AM10
GND	AM15
GND	AM2
GND	AM20
GND	AM25
GND	AM3
GND	AM31
GND	AM32
GND	AM33
GND	AM34
GND	AM4
GND	AN1
GND	AN2
GND	AN26
GND	AN3
GND	AN31
GND	AN32
GND	AN33
GND	AN34
GND	AN4
GND	AN9
GND	AP13
GND	AP2
GND	AP22
GND	AP27

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	AP3
GND	AP31
GND	AP32
GND	AP33
GND	AP4
GND	AP8
GND	B1
GND	B2
GND	B26
GND	B3
GND	B31
GND	B32
GND	B33
GND	B34
GND	B4
GND	B9
GND	C1
GND	C10
GND	C15
GND	C2
GND	C20
GND	C25
GND	C3
GND	C31
GND	C32
GND	C33
GND	C34
GND	C4
GND	D1
GND	D11
GND	D2
GND	D24
GND	D3
GND	D31
GND	D32
GND	D33
GND	D34

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	D4
GND	E12
GND	E17
GND	E18
GND	E23
GND	E30
GND	E5
GND	F29
GND	F30
GND	F6
GND	G28
GND	G6
GND	G7
GND	H1
GND	H34
GND	J2
GND	J33
GND	K3
GND	K32
GND	L11
GND	L24
GND	L31
GND	L4
GND	M12
GND	M23
GND	M30
GND	M5
GND	N1
GND	N13
GND	N22
GND	N34
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	P20
GND	P21
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R20
GND	R21
GND	R3
GND	R32
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T20
GND	T21
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	U20
GND	U21
GND	U30
GND	U5
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V20

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
GND	V21
GND	V30
GND	V5
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18
GND	W19
GND	W20
GND	W21
GND	Y14
GND	Y15
GND	Y16
GND	Y17
GND	Y18
GND	Y19
GND	Y20
GND	Y21
GND	Y3
GND	Y32
NC	A17
NC	A26
NC	AB2
NC	AB33
NC	AC34
NC	AD17
NC	AD3
NC	AD34
NC	AE18
NC	AE31
NC	AE33
NC	AE34
NC	AF1
NC	AF17
NC	AF18
NC	AF34

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
NC	AG2
NC	AG4
NC	AH1
NC	AH16
NC	AH19
NC	AH2
NC	AH31
NC	AH32
NC	AH34
NC	AJ1
NC	AJ2
NC	AJ3
NC	AJ31
NC	AJ32
NC	AJ33
NC	AJ34
NC	AJ4
NC	AK16
NC	AK19
NC	AL29
NC	AM19
NC	AM7
NC	AN13
NC	AN17
NC	AN25
NC	AN27
NC	AN8
NC	AP17
NC	AP9
NC	B17
NC	B22
NC	B27
NC	B8
NC	D10
NC	D20
NC	D23
NC	D25

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
NC	F3
NC	F32
NC	F33
NC	F34
NC	F4
NC	G1
NC	G32
NC	G33
NC	G34
NC	H16
NC	H19
NC	H31
NC	H33
NC	J1
NC	J16
NC	J19
NC	J3
NC	J34
NC	K17
NC	K18
NC	L17
NC	L18
NC	M1
NC	M4
NC	P1
NC	P2
NC	R31
NC	T1
NC	T2
NC	V3
NC	V34
NC	W3
NC	W34
PRA	J17
PRB	F18
PRC	AD18
PRD	AH18

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
TCK	J9
TDI	F7
TDO	L10
TMS	H8
TRST	E6
V_{CCA}	AA13
V_{CCA}	AA22
V_{CCA}	AB14
V_{CCA}	AB15
V_{CCA}	AB16
V_{CCA}	AB17
V_{CCA}	AB18
V_{CCA}	AB19
V_{CCA}	AB20
V_{CCA}	AB21
V_{CCA}	AF8
V_{CCA}	AK28
V_{CCA}	G30
V_{CCA}	G5
V_{CCA}	N14
V_{CCA}	N15
V_{CCA}	N16
V_{CCA}	N17
V_{CCA}	N18
V_{CCA}	N19
V_{CCA}	N20
V_{CCA}	N21
V_{CCA}	P13
V_{CCA}	P22
V_{CCA}	R13
V_{CCA}	R22
V_{CCA}	T13
V_{CCA}	T22
V_{CCA}	U13
V_{CCA}	U22
V_{CCA}	V13
V_{CCA}	V22

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
V_{CCA}	W13
V_{CCA}	W22
V_{CCA}	Y13
V_{CCA}	Y22
V_{CCDA}	AF26
V_{CCDA}	AF9
V_{CCDA}	AG17
V_{CCDA}	AG18
V_{CCDA}	AH14
V_{CCDA}	AH15
V_{CCDA}	AH17
V_{CCDA}	AH20
V_{CCDA}	AH21
V_{CCDA}	AK29
V_{CCDA}	AK6
V_{CCDA}	E15
V_{CCDA}	E29
V_{CCDA}	E7
V_{CCDA}	F15
V_{CCDA}	F21
V_{CCDA}	F5
V_{CCDA}	G20
V_{CCDA}	H17
V_{CCDA}	H18
V_{CCDA}	H28
V_{CCDA}	J18
V_{CCDA}	V27
V_{CCDA}	V6
$V_{CCI}B0$	A5
$V_{CCI}B0$	B5
$V_{CCI}B0$	C5
$V_{CCI}B0$	D5
$V_{CCI}B0$	L12
$V_{CCI}B0$	L13
$V_{CCI}B0$	L14
$V_{CCI}B0$	M13
$V_{CCI}B0$	M14

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B0$	M15
$V_{CCI}B0$	M16
$V_{CCI}B0$	M17
$V_{CCI}B1$	A30
$V_{CCI}B1$	B30
$V_{CCI}B1$	C30
$V_{CCI}B1$	D30
$V_{CCI}B1$	L21
$V_{CCI}B1$	L22
$V_{CCI}B1$	L23
$V_{CCI}B1$	M18
$V_{CCI}B1$	M19
$V_{CCI}B1$	M20
$V_{CCI}B1$	M21
$V_{CCI}B1$	M22
$V_{CCI}B2$	E31
$V_{CCI}B2$	E32
$V_{CCI}B2$	E33
$V_{CCI}B2$	E34
$V_{CCI}B2$	M24
$V_{CCI}B2$	N23
$V_{CCI}B2$	N24
$V_{CCI}B2$	P23
$V_{CCI}B2$	P24
$V_{CCI}B2$	R23
$V_{CCI}B2$	T23
$V_{CCI}B2$	U23
$V_{CCI}B3$	AA23
$V_{CCI}B3$	AA24
$V_{CCI}B3$	AB23
$V_{CCI}B3$	AB24
$V_{CCI}B3$	AC24
$V_{CCI}B3$	AK31
$V_{CCI}B3$	AK32
$V_{CCI}B3$	AK33
$V_{CCI}B3$	AK34
$V_{CCI}B3$	V23

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B3$	W23
$V_{CCI}B3$	Y23
$V_{CCI}B4$	AC18
$V_{CCI}B4$	AC19
$V_{CCI}B4$	AC20
$V_{CCI}B4$	AC21
$V_{CCI}B4$	AC22
$V_{CCI}B4$	AD21
$V_{CCI}B4$	AD22
$V_{CCI}B4$	AD23
$V_{CCI}B4$	AL30
$V_{CCI}B4$	AM30
$V_{CCI}B4$	AN30
$V_{CCI}B4$	AP30
$V_{CCI}B5$	AC13
$V_{CCI}B5$	AC14
$V_{CCI}B5$	AC15

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B5$	AC16
$V_{CCI}B5$	AC17
$V_{CCI}B5$	AD12
$V_{CCI}B5$	AD13
$V_{CCI}B5$	AD14
$V_{CCI}B5$	AL5
$V_{CCI}B5$	AM5
$V_{CCI}B5$	AN5
$V_{CCI}B5$	AP5
$V_{CCI}B6$	AA11
$V_{CCI}B6$	AA12
$V_{CCI}B6$	AB11
$V_{CCI}B6$	AB12
$V_{CCI}B6$	AC11
$V_{CCI}B6$	AK1
$V_{CCI}B6$	AK2
$V_{CCI}B6$	AK3

1152-Pin CCGA/LGA	
RTAX2000S/SL Function	**Pin Number**
$V_{CCI}B6$	AK4
$V_{CCI}B6$	V12
$V_{CCI}B6$	W12
$V_{CCI}B6$	Y12
$V_{CCI}B7$	E1
$V_{CCI}B7$	E2
$V_{CCI}B7$	E3
$V_{CCI}B7$	E4
$V_{CCI}B7$	M11
$V_{CCI}B7$	N11
$V_{CCI}B7$	N12
$V_{CCI}B7$	P11
$V_{CCI}B7$	P12
$V_{CCI}B7$	R12
$V_{CCI}B7$	T12
$V_{CCI}B7$	U12
V_{PUMP}	J26

1272-Pin CCGA/LGA

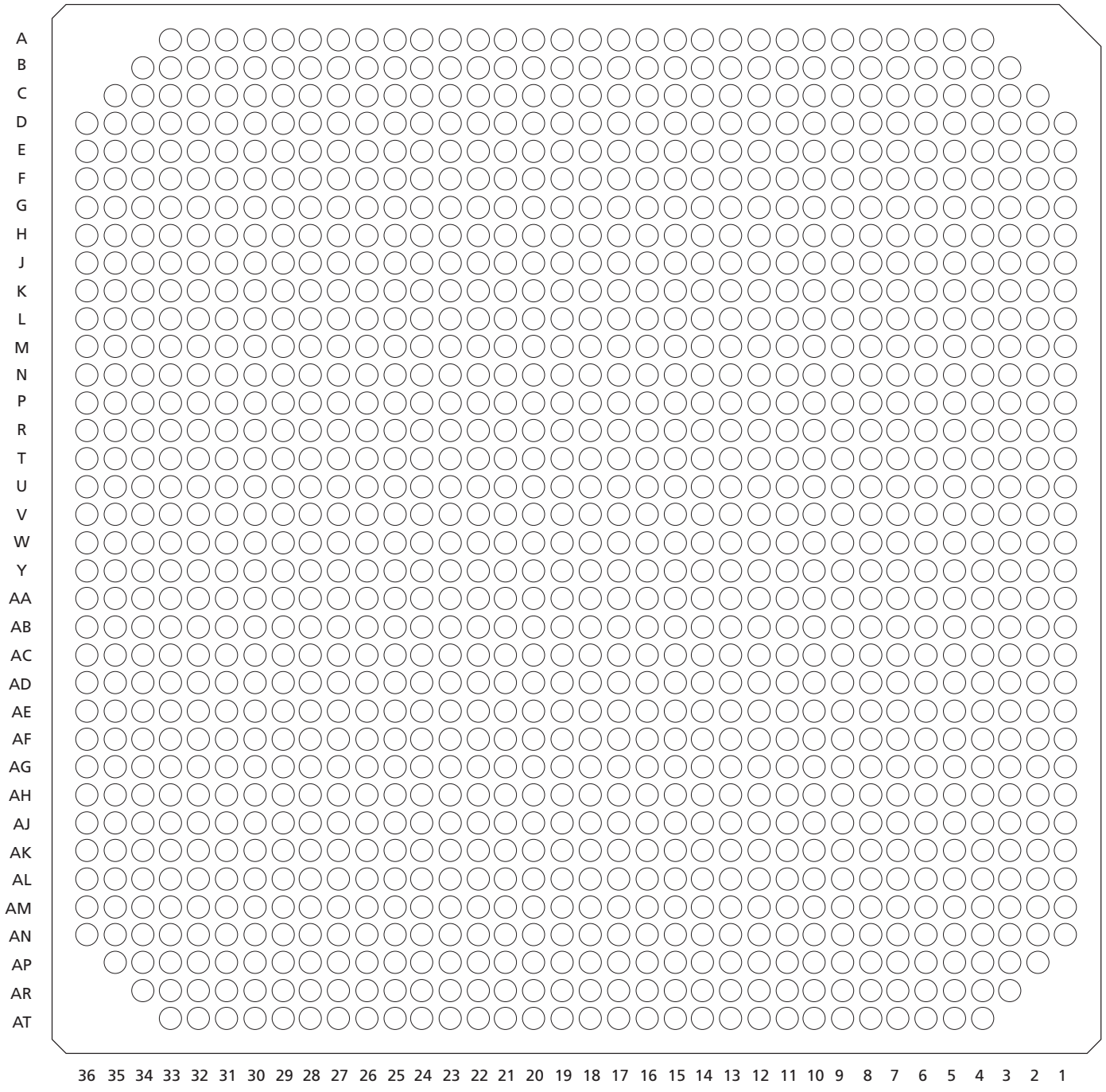


Figure 3-6 • **1272-Pin CCGA/LGA (Bottom View)**

Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/solutions/package/docs.aspx.

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
Bank 0	
IO00NB0F0	E9
IO00PB0F0	D9
IO01NB0F0	D8
IO01PB0F0	D7
IO02NB0F0	J10
IO02PB0F0	J9
IO03NB0F0	E7
IO03PB0F0	E8
IO04NB0F0	F9
IO04PB0F0	G9
IO05NB0F0	B7
IO05PB0F0	B6
IO06NB0F0	L13
IO06PB0F0	L12
IO07NB0F0	C7
IO07PB0F0	C6
IO08NB0F0	F10
IO08PB0F0	G10
IO09NB0F0	D10
IO09PB0F0	E10
IO10NB0F0	H11
IO10PB0F0	H10
IO11NB0F0	A5
IO11PB0F0	A4
IO12NB0F1	D6
IO12PB0F1	D5
IO13NB0F1	A7
IO13PB0F1	A6
IO14NB0F1	J12
IO14PB0F1	J11
IO15NB0F1	D12
IO15PB0F1	D11
IO16NB0F1	F12
IO16PB0F1	G12
IO17NB0F1	E12
IO17PB0F1	E11

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO18NB0F1	K13
IO18PB0F1	K12
IO19NB0F1	B4
IO19PB0F1	C4
IO20NB0F1	H13
IO20PB0F1	H12
IO21NB0F2	C13
IO21PB0F2	C12
IO22NB0F2	M14
IO22PB0F2	M13
IO23NB0F2	B10
IO23PB0F2	B9
IO24NB0F2	J14
IO24PB0F2	J13
IO25NB0F2	A8
IO25PB0F2	A9
IO26NB0F2	G13
IO26PB0F2	F13
IO27NB0F2	D14
IO27PB0F2	D13
IO28NB0F2	L16
IO28PB0F2	L15
IO29NB0F2	B13
IO29PB0F2	B12
IO30NB0F2	C10
IO30PB0F2	C9
IO31NB0F2	E15
IO31PB0F2	E14
IO32NB0F2	K15
IO32PB0F2	K16
IO33NB0F3	A13
IO33PB0F3	A12
IO34NB0F3	G15
IO34PB0F3	F15
IO35NB0F3	C15
IO35PB0F3	D15
IO36NB0F3	J16

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO36PB0F3	J15
IO37NB0F3	A11
IO37PB0F3	A10
IO38NB0F3	H15
IO38PB0F3	H14
IO39NB0F3	B16
IO39PB0F3	B15
IO40NB0F3	M16
IO40PB0F3	M17
IO41NB0F3	E16
IO41PB0F3	F16
IO42NB0F4	H17
IO42PB0F4	J17
IO43NB0F4	A14
IO43PB0F4	A15
IO44NB0F4	G16
IO44PB0F4	H16
IO45NB0F4	A17
IO45PB0F4	A16
IO46NB0F4	M18
IO46PB0F4	M19
IO47NB0F4	E18
IO47PB0F4	E17
IO48NB0F4	G18
IO48PB0F4	H18
IO49NB0F4	C18
IO49PB0F4	B18
IO50NB0F4/HCLKAN	J18
IO50PB0F4/HCLKAP	K18
IO51NB0F4/HCLKBN	D18
IO51PB0F4/HCLKBP	D17
Bank 1	
IO52NB1F6/HCLKCN	K19
IO52PB1F6/HCLKCP	J19
IO53NB1F6/HCLKDN	D20
IO53PB1F6/HCLKDP	D19
IO54NB1F6	H19

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO54PB1F6	G19
IO55NB1F6	B19
IO55PB1F6	C19
IO56NB1F6	M20
IO56PB1F6	M21
IO57NB1F6	E20
IO57PB1F6	E19
IO58NB1F6	H21
IO58PB1F6	G21
IO59NB1F6	A21
IO59PB1F6	A20
IO60NB1F7	H20
IO60PB1F7	J20
IO61NB1F7	A22
IO61PB1F7	A23
IO62NB1F7	D32
IO62PB1F7	D31
IO63NB1F7	F21
IO63PB1F7	E21
IO64NB1F7	J22
IO64PB1F7	J21
IO65NB1F7	B22
IO65PB1F7	B21
IO66NB1F7	H23
IO66PB1F7	H22
IO67NB1F7	D22
IO67PB1F7	C22
IO68NB1F7	K22
IO68PB1F7	K21
IO69NB1F7	A27
IO69PB1F7	A26
IO70NB1F7	F22
IO70PB1F7	G22
IO71NB1F7	E23
IO71PB1F7	E22
IO72NB1F8	L22
IO72PB1F8	L21

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO73NB1F8	A25
IO73PB1F8	A24
IO74NB1F8	C28
IO74PB1F8	C27
IO75NB1F8	D24
IO75PB1F8	D23
IO76NB1F8	J24
IO76PB1F8	J23
IO77NB1F8	B25
IO77PB1F8	B24
IO78NB1F8	F24
IO78PB1F8	G24
IO79NB1F8	A28
IO79PB1F8	A29
IO80NB1F8	M24
IO80PB1F8	M23
IO81NB1F8	B28
IO81PB1F8	B27
IO82NB1F9	H25
IO82PB1F9	H24
IO83NB1F9	C25
IO83PB1F9	C24
IO84NB1F9	K25
IO84PB1F9	K24
IO85NB1F9	A33
IO85PB1F9	A32
IO86NB1F9	G25
IO86PB1F9	F25
IO87NB1F9	E26
IO87PB1F9	E25
IO88NB1F9	J26
IO88PB1F9	J25
IO89NB1F9	D26
IO89PB1F9	D25
IO90NB1F9	E31
IO90PB1F9	E32
IO91NB1F9	A31

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO91PB1F9	A30
IO92NB1F9	H27
IO92PB1F9	H26
IO93NB1F9	C33
IO93PB1F9	B33
IO94NB1F10	G27
IO94PB1F10	F27
IO95NB1F10	E27
IO95PB1F10	D27
IO96NB1F10	L24
IO96PB1F10	L25
IO97NB1F10	C31
IO97PB1F10	C30
IO98NB1F10	F28
IO98PB1F10	G28
IO99NB1F10	B31
IO99PB1F10	B30
IO100NB1F10	J28
IO100PB1F10	J27
IO101NB1F10	E29
IO101PB1F10	E30
IO102NB1F10	D28
IO102PB1F10	E28
IO103NB1F10	D30
IO103PB1F10	D29
Bank 2	
IO104NB2F12	L29
IO104PB2F12	L28
IO105NB2F12	D35
IO105PB2F12	D34
IO106NB2F12	H33
IO106PB2F12	J33
IO107NB2F12	F34
IO107PB2F12	F33
IO108NB2F12	G33
IO108PB2F12	G32
IO109NB2F12	M28

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO109PB2F12	M27
IO110NB2F12	K33
IO110PB2F12	K32
IO111NB2F12	K31
IO111PB2F12	K30
IO112NB2F13	K34
IO112PB2F13	J34
IO113NB2F13	N26
IO113PB2F13	M26
IO114NB2F13	K28
IO114PB2F13	K29
IO115NB2F13	H32
IO115PB2F13	J32
IO116NB2F13	G35
IO116PB2F13	G34
IO117NB2F13	M29
IO117PB2F13	M30
IO118NB2F13	E33
IO118PB2F13	D33
IO119NB2F13	M32
IO119PB2F13	M31
IO120NB2F13	E36
IO120PB2F13	D36
IO121NB2F14	N28
IO121PB2F14	N27
IO122NB2F14	L33
IO122PB2F14	L32
IO123NB2F14	N30
IO123PB2F14	N29
IO124NB2F14	K35
IO124PB2F14	J35
IO125NB2F14	P25
IO125PB2F14	N25
IO126NB2F14	H36
IO126PB2F14	G36
IO127NB2F14	N32
IO127PB2F14	N31

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO128NB2F14	N34
IO128PB2F14	M34
IO129NB2F14	P29
IO129PB2F14	P28
IO130NB2F15	N33
IO130PB2F15	M33
IO131NB2F15	R26
IO131PB2F15	R25
IO132NB2F15	K36
IO132PB2F15	J36
IO133NB2F15	R29
IO133PB2F15	R28
IO134NB2F15	N35
IO134PB2F15	M35
IO135NB2F15	F35
IO135PB2F15	F36
IO136NB2F15	M36
IO136PB2F15	L36
IO137NB2F15	T26
IO137PB2F15	T25
IO138NB2F15	P33
IO138PB2F15	P32
IO139NB2F16	R31
IO139PB2F16	R30
IO140NB2F16	P36
IO140PB2F16	N36
IO141NB2F16	T28
IO141PB2F16	T27
IO142NB2F16	R35
IO142PB2F16	R34
IO143NB2F16	T32
IO143PB2F16	T31
IO144NB2F16	T35
IO144PB2F16	T34
IO145NB2F16	T30
IO145PB2F16	T29
IO146NB2F16	R33

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO146PB2F16	R32
IO147NB2F16	V25
IO147PB2F16	U25
IO148NB2F17	T36
IO148PB2F17	R36
IO149NB2F17	U29
IO149PB2F17	U28
IO150NB2F17	U33
IO150PB2F17	T33
IO151NB2F17	W25
IO151PB2F17	Y25
IO152NB2F17	V36
IO152PB2F17	U36
IO153NB2F17	V31
IO153PB2F17	V30
IO154NB2F17	V32
IO154PB2F17	U32
IO155NB2F17	V27
IO155PB2F17	V28
IO156NB2F17	W34
IO156PB2F17	V34
Bank 3	
IO157NB3F18	W29
IO157PB3F18	V29
IO158NB3F18	W35
IO158PB3F18	V35
IO159NB3F18	W30
IO159PB3F18	W31
IO160NB3F18	AA36
IO160PB3F18	Y36
IO161NB3F18	W27
IO161PB3F18	W28
IO162NB3F18	Y32
IO162PB3F18	W32
IO163NB3F18	Y28
IO163PB3F18	Y29
IO164NB3F18	AC36

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO164PB3F18	AB36
IO165NB3F18	AA26
IO165PB3F18	AA25
IO166NB3F19	AA33
IO166PB3F19	Y33
IO167NB3F19	AA32
IO167PB3F19	AA31
IO168NB3F19	AA34
IO168PB3F19	AA35
IO169NB3F19	AA29
IO169PB3F19	AA30
IO170NB3F19	AB32
IO170PB3F19	AB33
IO171NB3F19	AB31
IO171PB3F19	AB30
IO172NB3F19	AE36
IO172PB3F19	AD36
IO173NB3F19	AA27
IO173PB3F19	AA28
IO174NB3F19	AB34
IO174PB3F19	AB35
IO175NB3F20	AL35
IO175PB3F20	AL36
IO176NB3F20	AG36
IO176PB3F20	AF36
IO177NB3F20	AB25
IO177PB3F20	AB26
IO178NB3F20	AC32
IO178PB3F20	AC33
IO179NB3F20	AB29
IO179PB3F20	AB28
IO180NB3F20	AJ36
IO180PB3F20	AH36
IO181NB3F20	AC25
IO181PB3F20	AD25
IO182NB3F20	AE35
IO182PB3F20	AD35

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO183NB3F20	AC29
IO183PB3F20	AC28
IO184NB3F21	AE34
IO184PB3F21	AD34
IO185NB3F21	AE26
IO185PB3F21	AD26
IO186NB3F21	AE33
IO186PB3F21	AD33
IO187NB3F21	AD30
IO187PB3F21	AD29
IO188NB3F21	AH35
IO188PB3F21	AG35
IO189NB3F21	AD32
IO189PB3F21	AD31
IO190NB3F21	AK35
IO190PB3F21	AK36
IO191NB3F21	AE32
IO191PB3F21	AE31
IO192NB3F21	AN36
IO192PB3F21	AM36
IO193NB3F22	AD27
IO193PB3F22	AD28
IO194NB3F22	AF32
IO194PB3F22	AF33
IO195NB3F22	AE30
IO195PB3F22	AE29
IO196NB3F22	AK34
IO196PB3F22	AL34
IO197NB3F22	AE28
IO197PB3F22	AE27
IO198NB3F22	AN33
IO198PB3F22	AM33
IO199NB3F22	AH31
IO199PB3F22	AH30
IO200NB3F22	AH34
IO200PB3F22	AG34
IO201NB3F22	AF29

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO201PB3F22	AF28
IO202NB3F23	AG32
IO202PB3F23	AG33
IO203NB3F23	AG31
IO203PB3F23	AG30
IO204NB3F23	AL33
IO204PB3F23	AK33
IO205NB3F23	AK32
IO205PB3F23	AK31
IO206NB3F23	AH33
IO206PB3F23	AJ33
IO207NB3F23	AN34
IO207PB3F23	AN35
IO208NB3F23	AG29
IO208PB3F23	AG28
IO209NB3F23	AJ32
IO209PB3F23	AH32
Bank 4	
IO210NB4F24	AM28
IO210PB4F24	AN28
IO211NB4F24	AN29
IO211PB4F24	AN30
IO212NB4F24	AH27
IO212PB4F24	AH28
IO213NB4F24	AM30
IO213PB4F24	AM29
IO214NB4F24	AL28
IO214PB4F24	AK28
IO215NB4F24	AR30
IO215PB4F24	AR31
IO216NB4F24	AF24
IO216PB4F24	AF25
IO217NB4F24	AP30
IO217PB4F24	AP31
IO218NB4F24	AL27
IO218PB4F24	AK27
IO219NB4F24	AN27

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO219PB4F24	AM27
IO220NB4F25	AJ26
IO220PB4F25	AJ27
IO221NB4F25	AT32
IO221PB4F25	AT33
IO222NB4F25	AN31
IO222PB4F25	AN32
IO223NB4F25	AT30
IO223PB4F25	AT31
IO224NB4F25	AH25
IO224PB4F25	AH26
IO225NB4F25	AN25
IO225PB4F25	AN26
IO226NB4F25	AL25
IO226PB4F25	AK25
IO227NB4F25	AM25
IO227PB4F25	AM26
IO228NB4F25	AG25
IO228PB4F25	AG24
IO229NB4F25	AR33
IO229PB4F25	AP33
IO230NB4F25	AJ24
IO230PB4F25	AJ25
IO231NB4F25	AT26
IO231PB4F25	AT27
IO232NB4F26	AE23
IO232PB4F26	AE24
IO233NB4F26	AR27
IO233PB4F26	AR28
IO234NB4F26	AH23
IO234PB4F26	AH24
IO235NB4F26	AT29
IO235PB4F26	AT28
IO236NB4F26	AK24
IO236PB4F26	AL24
IO237NB4F26	AR24
IO237PB4F26	AR25

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO238NB4F26	AF21
IO238PB4F26	AF22
IO239NB4F26	AP24
IO239PB4F26	AP25
IO240NB4F26	AP27
IO240PB4F26	AP28
IO241NB4F26	AN23
IO241PB4F26	AN24
IO242NB4F27	AG21
IO242PB4F27	AG22
IO243NB4F27	AM22
IO243PB4F27	AM23
IO244NB4F27	AK22
IO244PB4F27	AL22
IO245NB4F27	AT24
IO245PB4F27	AT25
IO246NB4F27	AH21
IO246PB4F27	AH22
IO247NB4F27	AP22
IO247PB4F27	AN22
IO248NB4F27	AJ22
IO248PB4F27	AJ23
IO249NB4F27	AR21
IO249PB4F27	AR22
IO250NB4F27	AE21
IO250PB4F27	AE20
IO251NB4F27	AM21
IO251PB4F27	AL21
IO252NB4F27	AH20
IO252PB4F27	AJ20
IO253NB4F27	AT23
IO253PB4F27	AT22
IO254NB4F28	AK21
IO254PB4F28	AJ21
IO255NB4F28	AT20
IO255PB4F28	AT21
IO256NB4F28	AE18

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO256PB4F28	AE19
IO257NB4F28	AM19
IO257PB4F28	AM20
IO258NB4F28	AK19
IO258PB4F28	AJ19
IO259NB4F28	AP19
IO259PB4F28	AR19
IO260NB4F28/CLKEN	AH19
IO260PB4F28/CLKEP	AG19
IO261NB4F28/CLKFN	AN19
IO261PB4F28/CLKFP	AN20
Bank 5	
IO262NB5F30/CLKGN	AG18
IO262PB5F30/CLKGP	AH18
IO263NB5F30/CLKHN	AN17
IO263PB5F30/CLKHP	AN18
IO264NB5F30	AJ18
IO264PB5F30	AK18
IO265NB5F30	AR18
IO265PB5F30	AP18
IO266NB5F30	AE17
IO266PB5F30	AE16
IO267NB5F30	AM17
IO267PB5F30	AM18
IO268NB5F30	AJ16
IO268PB5F30	AK16
IO269NB5F30	AT16
IO269PB5F30	AT17
IO270NB5F30	AF16
IO270PB5F30	AF15
IO271NB5F30	AT15
IO271PB5F30	AT14
IO272NB5F31	AH17
IO272PB5F31	AJ17
IO273NB5F31	AL16
IO273PB5F31	AM16
IO274NB5F31	AH15

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO274PB5F31	AH16
IO275NB5F31	AR15
IO275PB5F31	AR16
IO276NB5F31	AJ14
IO276PB5F31	AJ15
IO277NB5F31	AN15
IO277PB5F31	AP15
IO278NB5F31	AG15
IO278PB5F31	AG16
IO279NB5F31	AT10
IO279PB5F31	AT11
IO280NB5F31	AL15
IO280PB5F31	AK15
IO281NB5F32	AM14
IO281PB5F32	AM15
IO282NB5F32	AE13
IO282PB5F32	AE14
IO283NB5F32	AT12
IO283PB5F32	AT13
IO284NB5F32	AP9
IO284PB5F32	AP10
IO285NB5F32	AN13
IO285PB5F32	AN14
IO286NB5F32	AN9
IO286PB5F32	AM9
IO287NB5F32	AR12
IO287PB5F32	AR13
IO288NB5F32	AL13
IO288PB5F32	AK13
IO289NB5F32	AT9
IO289PB5F32	AT8
IO290NB5F32	AH13
IO290PB5F32	AH14
IO291NB5F32	AR9
IO291PB5F32	AR10
IO292NB5F32	AJ12
IO292PB5F32	AJ13

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO293NB5F33	AP12
IO293PB5F33	AP13
IO294NB5F33	AG13
IO294PB5F33	AF13
IO295NB5F33	AP4
IO295PB5F33	AR4
IO296NB5F33	AG12
IO296PB5F33	AF12
IO297NB5F33	AM11
IO297PB5F33	AM12
IO298NB5F33	AK12
IO298PB5F33	AL12
IO299NB5F33	AN11
IO299PB5F33	AN12
IO300NB5F33	AN5
IO300PB5F33	AN6
IO301NB5F33	AT6
IO301PB5F33	AT7
IO302NB5F34	AH11
IO302PB5F34	AH12
IO303NB5F34	AT4
IO303PB5F34	AT5
IO304NB5F34	AJ10
IO304PB5F34	AJ11
IO305NB5F34	AM10
IO305PB5F34	AN10
IO306NB5F34	AK10
IO306PB5F34	AL10
IO307NB5F34	AP6
IO307PB5F34	AP7
IO308NB5F34	AK9
IO308PB5F34	AL9
IO309NB5F34	AR6
IO309PB5F34	AR7
IO310NB5F34	AH9
IO310PB5F34	AH10
IO311NB5F34	AM8

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO311PB5F34	AM7
IO312NB5F34	AG9
IO312PB5F34	AG8
IO313NB5F34	AN7
IO313PB5F34	AN8
Bank 6	
IO314NB6F36	AF8
IO314PB6F36	AF9
IO315NB6F36	AN2
IO315PB6F36	AN3
IO316NB6F36	AH4
IO316PB6F36	AJ4
IO317NB6F36	AL3
IO317PB6F36	AL4
IO318NB6F36	AK4
IO318PB6F36	AK5
IO319NB6F36	AE10
IO319PB6F36	AE9
IO320NB6F36	AG4
IO320PB6F36	AG5
IO321NB6F36	AE11
IO321PB6F36	AD11
IO322NB6F37	AG3
IO322PB6F37	AH3
IO323NB6F37	AG7
IO323PB6F37	AG6
IO324NB6F37	AH7
IO324PB6F37	AH6
IO325NB6F37	AJ5
IO325PB6F37	AH5
IO326NB6F37	AK2
IO326PB6F37	AK3
IO327NB6F37	AE7
IO327PB6F37	AE8
IO328NB6F37	AM4
IO328PB6F37	AN4
IO329NB6F37	AD9

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO329PB6F37	AD10
IO330NB6F37	AM1
IO330PB6F37	AN1
IO331NB6F38	AE5
IO331PB6F38	AE6
IO332NB6F38	AF4
IO332PB6F38	AF5
IO333NB6F38	AD8
IO333PB6F38	AD7
IO334NB6F38	AG2
IO334PB6F38	AH2
IO335NB6F38	AC12
IO335PB6F38	AD12
IO336NB6F38	AJ1
IO336PB6F38	AK1
IO337NB6F38	AC8
IO337PB6F38	AC9
IO338NB6F38	AD3
IO338PB6F38	AE3
IO339NB6F38	AD5
IO339PB6F38	AD6
IO340NB6F39	AD4
IO340PB6F39	AE4
IO341NB6F39	AB8
IO341PB6F39	AB9
IO342NB6F39	AG1
IO342PB6F39	AH1
IO343NB6F39	AA12
IO343PB6F39	AB12
IO344NB6F39	AD2
IO344PB6F39	AE2
IO345NB6F39	AA11
IO345PB6F39	AB11
IO346NB6F39	AE1
IO346PB6F39	AF1
IO347NB6F39	AL1
IO347PB6F39	AL2

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO348NB6F39	AC4
IO348PB6F39	AC5
IO349NB6F40	AB6
IO349PB6F40	AB7
IO350NB6F40	AC1
IO350PB6F40	AD1
IO351NB6F40	AA9
IO351PB6F40	AA10
IO352NB6F40	AB2
IO352PB6F40	AB3
IO353NB6F40	AA7
IO353PB6F40	AA8
IO354NB6F40	AA2
IO354PB6F40	AA3
IO355NB6F40	AA5
IO355PB6F40	AA6
IO356NB6F40	AB4
IO356PB6F40	AB5
IO357NB6F40	W12
IO357PB6F40	Y12
IO358NB6F41	AA1
IO358PB6F41	AB1
IO359NB6F41	Y8
IO359PB6F41	Y9
IO360NB6F41	Y4
IO360PB6F41	AA4
IO361NB6F41	U12
IO361PB6F41	V12
IO362NB6F41	W1
IO362PB6F41	Y1
IO363NB6F41	W6
IO363PB6F41	W7
IO364NB6F41	W5
IO364PB6F41	Y5
IO365NB6F41	W10
IO365PB6F41	W9
IO366NB6F41	V2

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO366PB6F41	W2
Bank 7	
IO367NB7F42	V8
IO367PB7F42	W8
IO368NB7F42	V3
IO368PB7F42	W3
IO369NB7F42	V9
IO369PB7F42	V10
IO370NB7F42	U1
IO370PB7F42	V1
IO371NB7F42	V7
IO371PB7F42	V6
IO372NB7F42	U5
IO372PB7F42	V5
IO373NB7F42	U9
IO373PB7F42	U8
IO374NB7F42	R1
IO374PB7F42	T1
IO375NB7F42	T11
IO375PB7F42	T12
IO376NB7F43	T4
IO376PB7F43	U4
IO377NB7F43	T8
IO377PB7F43	T7
IO378NB7F43	T3
IO378PB7F43	T2
IO379NB7F43	T5
IO379PB7F43	T6
IO380NB7F43	R5
IO380PB7F43	R4
IO381NB7F43	R6
IO381PB7F43	R7
IO382NB7F43	N1
IO382PB7F43	P1
IO383NB7F43	T10
IO383PB7F43	T9
IO384NB7F43	R3

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO384PB7F43	R2
IO385NB7F44	R12
IO385PB7F44	R11
IO386NB7F44	L1
IO386PB7F44	M1
IO387NB7F44	G2
IO387PB7F44	F2
IO388NB7F44	P5
IO388PB7F44	P4
IO389NB7F44	R8
IO389PB7F44	R9
IO390NB7F44	J1
IO390PB7F44	K1
IO391NB7F44	N12
IO391PB7F44	P12
IO392NB7F44	M2
IO392PB7F44	N2
IO393NB7F44	P9
IO393PB7F44	P8
IO394NB7F45	M3
IO394PB7F45	N3
IO395NB7F45	M11
IO395PB7F45	N11
IO396NB7F45	M4
IO396PB7F45	N4
IO397NB7F45	N5
IO397PB7F45	N6
IO398NB7F45	J2
IO398PB7F45	K2
IO399NB7F45	N8
IO399PB7F45	N7
IO400NB7F45	G1
IO400PB7F45	H1
IO401NB7F45	M5
IO401PB7F45	M6
IO402NB7F45	E1
IO402PB7F45	F1

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
IO403NB7F46	N10
IO403PB7F46	N9
IO404NB7F46	L5
IO404PB7F46	L4
IO405NB7F46	M7
IO405PB7F46	M8
IO406NB7F46	G3
IO406PB7F46	F3
IO407NB7F46	M10
IO407PB7F46	M9
IO408NB7F46	D4
IO408PB7F46	D3
IO409NB7F46	J7
IO409PB7F46	J6
IO410NB7F46	J3
IO410PB7F46	K3
IO411NB7F46	L8
IO411PB7F46	L9
IO412NB7F47	K5
IO412PB7F47	K4
IO413NB7F47	K7
IO413PB7F47	K6
IO414NB7F47	E4
IO414PB7F47	F4
IO415NB7F47	G4
IO415PB7F47	G5
IO416NB7F47	H4
IO416PB7F47	J4
IO417NB7F47	D2
IO417PB7F47	D1
IO418NB7F47	K8
IO418PB7F47	K9
IO419NB7F47	H5
IO419PB7F47	J5
Dedicated I/O	
GND	J8
GND	AA13

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
GND	AA15
GND	AA17
GND	AA19
GND	AA21
GND	AA23
GND	AA24
GND	AB14
GND	AB16
GND	AB18
GND	AB20
GND	AB22
GND	AC11
GND	AC13
GND	AC15
GND	AC17
GND	AC19
GND	AC21
GND	AC23
GND	AC24
GND	AC26
GND	AC3
GND	AC30
GND	AC34
GND	AC7
GND	AD13
GND	AD14
GND	AD16
GND	AD18
GND	AD19
GND	AD21
GND	AD23
GND	AD24
GND	AE15
GND	AE25
GND	AF10
GND	AF11
GND	AF14

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	Pin Number
GND	AF17
GND	AF20
GND	AF23
GND	AF26
GND	AF27
GND	AF3
GND	AF30
GND	AF34
GND	AF7
GND	AJ29
GND	AJ3
GND	AJ30
GND	AJ34
GND	AJ7
GND	AK11
GND	AK14
GND	AK17
GND	AK20
GND	AK23
GND	AK26
GND	AK29
GND	AK6
GND	AK8
GND	AL18
GND	AL31
GND	AL7
GND	AM3
GND	AM34
GND	AP11
GND	AP14
GND	AP17
GND	AP2
GND	AP20
GND	AP23
GND	AP26
GND	AP29
GND	AP32

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	Pin Number
GND	AP35
GND	AP5
GND	AP8
GND	AR3
GND	AR34
GND	B3
GND	B34
GND	C11
GND	C14
GND	C17
GND	C2
GND	C20
GND	C23
GND	C26
GND	C29
GND	C32
GND	C35
GND	C5
GND	C8
GND	E3
GND	E34
GND	F30
GND	F7
GND	G11
GND	G14
GND	G17
GND	G20
GND	G23
GND	G26
GND	G29
GND	G8
GND	H3
GND	H30
GND	H34
GND	H7
GND	J31
GND	L10

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	Pin Number
GND	L11
GND	L14
GND	L17
GND	L20
GND	L23
GND	L26
GND	L27
GND	L3
GND	L30
GND	L34
GND	L7
GND	M15
GND	M25
GND	N14
GND	N16
GND	N18
GND	N19
GND	N21
GND	N23
GND	N24
GND	P11
GND	P13
GND	P14
GND	P16
GND	P18
GND	P20
GND	P22
GND	P24
GND	P26
GND	P3
GND	P30
GND	P34
GND	P7
GND	R15
GND	R17
GND	R19
GND	R21

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
GND	R23
GND	R27
GND	T13
GND	T14
GND	T16
GND	T18
GND	T20
GND	T22
GND	T24
GND	U11
GND	U15
GND	U17
GND	U19
GND	U21
GND	U23
GND	U26
GND	U3
GND	U30
GND	U34
GND	U7
GND	V13
GND	V14
GND	V16
GND	V18
GND	V20
GND	V22
GND	V24
GND	V33
GND	V4
GND	W11
GND	W13
GND	W15
GND	W17
GND	W19
GND	W21
GND	W23
GND	W24

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
GND	W26
GND	W4
GND	Y11
GND	Y14
GND	Y16
GND	Y18
GND	Y20
GND	Y22
GND	Y26
GND	Y3
GND	Y30
GND	Y34
GND	Y7
NC	AJ8
NC	W36
PRA	F18
PRB	A18
PRC	AL19
PRD	AT19
TCK	H8
TDI	F6
TDO	H9
TMS	F5
TRST	G7
V_{CCA}	A19
V_{CCA}	AA14
V_{CCA}	AA16
V_{CCA}	AA18
V_{CCA}	AA20
V_{CCA}	AA22
V_{CCA}	AB15
V_{CCA}	AB17
V_{CCA}	AB19
V_{CCA}	AB21
V_{CCA}	AB23
V_{CCA}	AC14
V_{CCA}	AC16

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
V_{CCA}	AC18
V_{CCA}	AC20
V_{CCA}	AC22
V_{CCA}	AE12
V_{CCA}	AL32
V_{CCA}	AL5
V_{CCA}	AP3
V_{CCA}	AP34
V_{CCA}	AT18
V_{CCA}	C3
V_{CCA}	C34
V_{CCA}	J30
V_{CCA}	M12
V_{CCA}	P15
V_{CCA}	P17
V_{CCA}	P19
V_{CCA}	P21
V_{CCA}	P23
V_{CCA}	R14
V_{CCA}	R16
V_{CCA}	R18
V_{CCA}	R20
V_{CCA}	R22
V_{CCA}	T15
V_{CCA}	T17
V_{CCA}	T19
V_{CCA}	T21
V_{CCA}	T23
V_{CCA}	U14
V_{CCA}	U16
V_{CCA}	U18
V_{CCA}	U20
V_{CCA}	U22
V_{CCA}	V15
V_{CCA}	V17
V_{CCA}	V19
V_{CCA}	V21

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
V_{CCA}	V23
V_{CCA}	W14
V_{CCA}	W16
V_{CCA}	W18
V_{CCA}	W20
V_{CCA}	W22
V_{CCA}	W33
V_{CCA}	Y15
V_{CCA}	Y17
V_{CCA}	Y19
V_{CCA}	Y21
V_{CCA}	Y23
V_{CCDA}	AB10
V_{CCDA}	AB27
V_{CCDA}	AE22
V_{CCDA}	AF18
V_{CCDA}	AF19
V_{CCDA}	AH29
V_{CCDA}	AH8
V_{CCDA}	AJ28
V_{CCDA}	AJ9
V_{CCDA}	AK30
V_{CCDA}	AK7
V_{CCDA}	AL30
V_{CCDA}	AL6
V_{CCDA}	AM13
V_{CCDA}	AM24
V_{CCDA}	AM31
V_{CCDA}	AM32
V_{CCDA}	AM5
V_{CCDA}	AM6
V_{CCDA}	AN16
V_{CCDA}	AN21
V_{CCDA}	AP16
V_{CCDA}	AP21
V_{CCDA}	C16
V_{CCDA}	C21

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
V_{CCDA}	D16
V_{CCDA}	D21
V_{CCDA}	E13
V_{CCDA}	E24
V_{CCDA}	E5
V_{CCDA}	E6
V_{CCDA}	F19
V_{CCDA}	F31
V_{CCDA}	G30
V_{CCDA}	G31
V_{CCDA}	G6
V_{CCDA}	H28
V_{CCDA}	H29
V_{CCDA}	J29
V_{CCDA}	L18
V_{CCDA}	L19
V_{CCDA}	M22
V_{CCDA}	N13
V_{CCDA}	R10
V_{CCDA}	V11
V_{CCDA}	V26
$V_{CCI}B0$	B11
$V_{CCI}B0$	B14
$V_{CCI}B0$	B17
$V_{CCI}B0$	B5
$V_{CCI}B0$	B8
$V_{CCI}B0$	F11
$V_{CCI}B0$	F14
$V_{CCI}B0$	F17
$V_{CCI}B0$	F8
$V_{CCI}B0$	K11
$V_{CCI}B0$	K14
$V_{CCI}B0$	K17
$V_{CCI}B0$	N15
$V_{CCI}B0$	N17
$V_{CCIB}1$	B20
$V_{CCIB}1$	B23

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
$V_{CCIB}1$	B26
$V_{CCIB}1$	B29
$V_{CCIB}1$	B32
$V_{CCIB}1$	F20
$V_{CCIB}1$	F23
$V_{CCIB}1$	F26
$V_{CCIB}1$	F29
$V_{CCIB}1$	K20
$V_{CCIB}1$	K23
$V_{CCIB}1$	K26
$V_{CCIB}1$	N20
$V_{CCIB}1$	N22
$V_{CCI}B2$	E35
$V_{CCI}B2$	H31
$V_{CCI}B2$	H35
$V_{CCI}B2$	K27
$V_{CCI}B2$	L31
$V_{CCI}B2$	L35
$V_{CCI}B2$	P27
$V_{CCI}B2$	P31
$V_{CCI}B2$	P35
$V_{CCI}B2$	R24
$V_{CCI}B2$	U24
$V_{CCI}B2$	U27
$V_{CCI}B2$	U31
$V_{CCI}B2$	U35
$V_{CCI}B3$	AB24
$V_{CCI}B3$	AC27
$V_{CCI}B3$	AC31
$V_{CCI}B3$	AC35
$V_{CCI}B3$	AF31
$V_{CCI}B3$	AF35
$V_{CCI}B3$	AG27
$V_{CCI}B3$	AJ31
$V_{CCI}B3$	AJ35
$V_{CCI}B3$	AM35
$V_{CCI}B3$	Y24

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
$V_{CCI}B3$	Y27
$V_{CCI}B3$	Y31
$V_{CCI}B3$	Y35
$V_{CCI}B4$	AD20
$V_{CCI}B4$	AD22
$V_{CCI}B4$	AG20
$V_{CCI}B4$	AG23
$V_{CCI}B4$	AG26
$V_{CCI}B4$	AL20
$V_{CCI}B4$	AL23
$V_{CCI}B4$	AL26
$V_{CCI}B4$	AL29
$V_{CCI}B4$	AR20
$V_{CCI}B4$	AR23
$V_{CCI}B4$	AR26
$V_{CCI}B4$	AR29
$V_{CCI}B4$	AR32
$V_{CCI}B5$	AD15
$V_{CCI}B5$	AD17
$V_{CCI}B5$	AG11

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
$V_{CCI}B5$	AG14
$V_{CCI}B5$	AG17
$V_{CCI}B5$	AL11
$V_{CCI}B5$	AL14
$V_{CCI}B5$	AL17
$V_{CCI}B5$	AL8
$V_{CCI}B5$	AR11
$V_{CCI}B5$	AR14
$V_{CCI}B5$	AR17
$V_{CCI}B5$	AR5
$V_{CCI}B5$	AR8
$V_{CCI}B6$	AB13
$V_{CCI}B6$	AC10
$V_{CCI}B6$	AC2
$V_{CCI}B6$	AC6
$V_{CCI}B6$	AF2
$V_{CCI}B6$	AF6
$V_{CCI}B6$	AG10
$V_{CCI}B6$	AJ2
$V_{CCI}B6$	AJ6

1272-Pin CCGA/LGA	
RTAX4000S/SL Function	**Pin Number**
$V_{CCI}B6$	AM2
$V_{CCI}B6$	Y10
$V_{CCI}B6$	Y13
$V_{CCI}B6$	Y2
$V_{CCI}B6$	Y6
$V_{CCI}B7$	E2
$V_{CCI}B7$	H2
$V_{CCI}B7$	H6
$V_{CCI}B7$	K10
$V_{CCI}B7$	L2
$V_{CCI}B7$	L6
$V_{CCI}B7$	P10
$V_{CCI}B7$	P2
$V_{CCI}B7$	P6
$V_{CCI}B7$	R13
$V_{CCI}B7$	U10
$V_{CCI}B7$	U13
$V_{CCI}B7$	U2
$V_{CCI}B7$	U6
V_{PUMP}	F32

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v5.4)	Page
v5.3 (October 2008)	RT4000S now supports the low-power grade option. In addition, this device has moved from a preliminary state to a production state.	N/A
	RTAX250S/SL supports 624-CCGA/LGA. The following tables were updated. "RTAX-S/SL Family Product Profile","Temperature Grade Offerings","Ordering Information"	N/A
	All DC input and output tables and timing characteristic tables were updated.	N/A
	The "Ordering Information" section was updated. B was deleted from the Package Type and the speed grade description was updated.	ii
	The "Temperature Grade Offerings" table note was updated.	ii
	The "Speed Grade and Temperature Grade Matrix" table was updated.	iii
	The "I/Os per Package" table is new.	iii
	In Table 2 • Actel MIL-STD-883 Class B Product Flow for RTAX-S/SL1, 2, "TBD" in step 4 was changed to "Condition A".	iv
	In Table 3 • Actel Extended Flow for RTAX-S/SL1, 2, 3, 4, "TBD" in step 4 was changed to "Condition A".	v
	In the first paragraph of the "General Description" section, it originally said there were two million equivalent system gates but that is incorrect because there are four million equivalent system gates.	1-1
	Information about segmenting clocks was added to the "Global Resources" section.	1-7
	The "Prototyping with ProASIC3E Reprogrammable Units" section is new.	1-8
	In Table 2-1 • I/O Features Comparison, LVTTL was updated. Note 1 was updated and note 4 is new.	2-1
	In Table 2-2 • Absolute Maximum Ratings, the limit for V_I was changed from 4.0 to 4.1 and V_{PUMP} was added to the table.	2-2
	The "5 V Tolerance" section was significantly updated.	2-1
	RTAX4000S/SL data was updated in Table 2-4 • RTAX-S Standby Current. For RTAX2000S/SL, $I_{CCDIFFA}$ was changed from 2.96 to 3.13. The I_{IL}/I_{IH} heading was changed to I_{IH}, I_{IL}, or I_{OZ}. Note 1 is new.	2-3
	RTAX4000S/SL data was added to Table 2-5 • RTAX-SL Standby Current. I_{CCA} data was updated for Typical 25°C for RTAX2000S/SL, RTAX1000S/SL, and RTAX250S/SL. The I_{IL}/I_{IH} heading was changed to I_{IH}, I_{IL}, or I_{OZ}. Note 1 is new.	2-3
	Table 2-6 • Default Cload / VCCI was significantly updated.	2-4
	In the "Ptotal = Pdc + Pac" section, the "Pdc" definition, N_{banks} was deleted.	2-5
	In the "Pmemory = 0 mW" section, the "Pdc" definition, N_{banks} was deleted.	2-6
	Table 2-8 • Package Thermal Characteristics was updated to include 624-pin CCGA/LGA	2-7
	Table 2-9 • Temperature and Voltage Timing Derating Factors was significantly updated.	2-9
	In the "Hardwired Clock" section, the Clock-to-Out (Pad-to-Pad) was updated. T_{RCO} was changed from 0.9 to 0.96.	2-10
	In the "Routed Clock1" section, the Clock-to-Out (Pad-to-Pad) was updated. T_{RCO} was changed from 0.9 to 0.96. Footnote 1 is new.	2-10
	The "VCCIBx Supply Voltage" section was updated to include information about unused banks.	2-11
	The "HCLKA/B/C/D Dedicated (Hardwired) Clocks A, B, C, and D" section was updated.	2-11
	The "VPUMP Supply Voltage (External Pump)" section was updated.	2-11

Previous version	Changes in current version (v5.4)	Page
v5.3 (continued)	The "CLKE/F/G/H Global Clocks E, F, G, and H" section was updated.	2-11
	The "PRA/B/C/D Probes A, B, C, and D" section was updated.	2-12
	Information about SEUs and cell buffers was added to "Introduction" section.	2-12
	In Table 2-15 • Macros for Single-Ended I/O Standards, the macro names for LVTTL were changed from _H_ to _F_	2-19
	The "Customizing the I/O" section was updated. Table 2-14 • Bank Wide Delay Values is new.	2-14
	The data in Table 2-19 • I/O Weak Pull-Up/Pull-Down Resistances1 was significantly updated. Notes 1, 2, and 3 were also updated.	2-22
	The note was updated to include pin compatibility information for "352-Pin CQFP".	3-8
	The note was updated to include pin compatibility information for "624-Pin CCGA/LGA". the RTAX250S/SL pin table is new.	3-26
	The "352-Pin CQFP" table for the RTAX250S/SL device is new.	3-10
	In Table 2-21 • DC Input and Output Levels, the footnote is new.	2-26
	In Table 2-36 • Worst-Case Military Conditions VCCA = 1.4 V, VCCI = 3.0 V, TJ = 125°C, the footnote is new.	2-51
	Table 2-54 • Worst-Case Military Conditions VCCA = 1.4 V, VCCI = 3.0 V, TJ = 125°C was significantly updated.	2-57
	Table 2-88 • One RAM Block (Worst-Case Military Conditions VCCA = 1.4 V, VCCI = 3.0 V, TJ = 125°C) to Table 2-92 • Sixteen RAM Blocks Are Cascaded (Worst-Case Military Conditions VCCA = 1.4 V, VCCI = 3.0 V, TJ = 125°C) were updated.	2-85 to 2-89
	Table 2-96 • FIFO Signal Description to Table 2-101 • Sixteen FIFO Blocks are Cascaded (Worst-Case MIlitary Conditions VCCA = 1.4 V, VCCI = 3.0 V, TJ = 125°C) were updated.	2-94 to 2-98
	In the "RTAX2000S/SL Function" table, the block numbers were removed. For example "Bank 0, Block 0" was changed to "Bank 0".	3-5
v5.2 (October 2007)	In Table 2-5 • RTAX-SL Standby Current, the I_{CCA} specifications were updated for 125°C.	2-3
v5.1 (August 2007)	The "I/O Logic" section was updated to include information about user flip-flops being immune to SEU.	1-5
	The "Low-Cost Prototyping Solutions" section was updated significantly.	1-7
	Table 2-4 • RTAX-S Standby Current was updated to include I_{IH}/I_{IL}.	2-3
	Table 2-5 • RTAX-SL Standby Current was updated to include I_{IH}/I_{IL}.	2-3
	The CG1272 was updated in the "Package Thermal Characteristics" table.	2-7
	The temperature in note 1 was changed from 175 to 125 in the "Temperature and Voltage Timing Derating Factors" table.	2-9
	In the "Timing Model", the Hardwired Clock was changed to Routed or Hardwired.	2-10
v5.0 (June 2007)	The "Ordering Information" section was updated to include the Sigma Six Column and BAE Column designation. A note was added to the "Temperature Grade Offerings" table regarding the Sigma Six Column and BAE Column.	ii

Previous version	Changes in current version (v5.4)	Page
v4.0 (May 2007)	RTAX-SL information is new.	N/A
	EV Flow (Class V Flow Equivalent Processing) information is new.	N/A
	The "Ordering Information" section was updated.	ii
	The "Actel MIL-STD-883 Class B Product Flow" table was updated.	iv
	The "Actel Extended Flow" table was updated.	v
	The "Low-Cost Prototyping Solutions" section was updated to include RTAX-SL prototyping information.	1-7
	Table 2-5 • RTAX-SL Standby Current is new.	2-3
	In the "Sample Case 2: Convection = 0" section, θ_{cb} was changed to T_j.	2-8
	The Axcelerator figure listed below the "VCCDA Supply Voltage" section was incorrect and has been removed from the datasheet.	2-11
	The "256-Pin CQFP" table for the RTAX2000S/SL device is new.	3-5
v3.0 September 2006	All information regarding the RTAX4000S device is new.	N/A
	The "Timing Model" was updated.	2-10
	The "Specifications" section was updated.	i
	The SEL and SET information was updated in the "Designed for Space" section.	i
	The maximum I/O counts for the RTAX250S and RTAX1000S were updated in Table 1 • RTAX-S/SL Family Product Profile.	i
	The "Device Resources" table was updated for CG1272/LG1272.	iii
	The ***RTAX-S/SL Testing and Reliability Update*** white paper was added to the "White Papers" section.	1-9
	The "User I/Os" section was updated with information on configuring unused I/Os.	2-12
	Implementing DDR was updated in the "Using DDR (Double Data Rate)" section.	2-17
	PSET was changed to PRE and D was changed to E in Figure 2-6 • DDR Register.	2-18
v3.0 (continued)	The "JTAG" section was updated with JTAG pin information.	2-100
	Figure 2-1 • Use of an External Resistor for 5 V Tolerance was updated.	2-1
	Note 2 in Table 2-2 • Absolute Maximum Ratings was updated.	2-2
	The "Calculating Power Dissipation" section was updated.	2-3
	Table 2-25 • Worst-Case Military Conditions VCCA = 1.4 V, VCCI = 2.3 V, TJ = 125°C was updated.	2-30
	The "Hardwired Clock" and "Routed Clock1" equations were updated.	2-10
	Table 2-4 • RTAX-S Standby Current was updated.	2-3
	Table 2-6 • Default Cload / VCCI was updated.	2-4
	Table 2-9 • Temperature and Voltage Timing Derating Factors was updated.	2-9
	All timing characteristic tables were updated.	N/A
	The "352-Pin CQFP" table for the RTAX4000S is new.	3-22
	The "1272-Pin CCGA/LGA" table for the RTAX4000S is new.	3-58
v2.2 May 2006	All Timing Characteristic tables were updated.	N/A
	Cold Sparing was added to the Hot Insertion heading in Table 2-1 • I/O Features Comparison.	2-1
	The "Thermal Characteristics" section was updated.	2-7
	The "Simultaneous Switching Outputs (SSO)" section was updated.	2-14
	The "Timing Model" has been updated.	2-10

Previous version	Changes in current version (v5.4)	Page
v2.2 (continued)	The "Hardwired Clock" and "Routed Clock1" equations were updated.	2-10
	Table 2-6 • Default Cload / VCCI was updated.	2-4
	Table 2-18 • I/O Weak Pull-Up/Pull-Down Resistances[1] is new.	2-21
	A note was added to Table 2-58 • DC Input and Output Levels.	2-60
v2.1 October 2005	The LVDS Capable I/O specification was added to "Leading-Edge Performance".	i-i
	Table 1 • RTAX-S/SL Family Product Profile was updated to include CQ256.	i-i
	CQ256 was added to the"Temperature Grade Offerings" table.	i-ii
	CQ256 is new and CQ352 for the RTAX1000S device was updated in the "Device Resources" table.	i-iii
	The "Overshoot/Undershoot Limits" section is new.	2-2
	Table 2-2 • Absolute Maximum Ratings was updated.	2-2
	Table 2-3 • RTAX-S/SL Recommended Operating Conditions was updated.	2-2
	The "Timing Model" has been updated.	2-10
	The "Hardwired Clock" and "Routed Clock1" equations were updated.	2-10
	This sentence was updated in the "CLKE/F/G/H Global Clocks E, F, G, and H" section: When the CLK pins are unused, Actel recommends that they are tied to a known state.	2-11
	Figure 2-27 • LVPECL Circuit was updated. The following labels were corrected: INBUF_LVPECL OUTBUF_LVPECL	2-60
	The following sentence was removed from "Global Resource Distribution": An unused input can be tied to ground for power savings.	2-78
	The "RAM" section was updated.	2-81
	The "256-Pin CQFP" package figure and is new.	3-4
v2.0	In Table 2-4, the I_{CCA} column heading was changed to I_{CCDA} and note 3 is new.	2-3

Previous version	Changes in current version (v5.4)	Page
Advanced v0.5	The "Designed for Space" section was updated.	i-i
	Table 1 was updated to include 1152 CCGA/LGA.	i-i
	The "Temperature Grade Offerings" table was updated to include the 1152 CCGA.	i-iii
	The RTAX1000S and the RTAX2000S columns were updated in the "Device Resources" table.	i-iii
	Figure 1-9 was updated and a note was added to the figure.	1-8
	Table 2-4 • RTAX-S Standby Current was updated.	2-3
	In Table 2-4 the LVPECL and LVDS specifications were updated. A note was also added to the table.	2-3
	The "Global Resource Access Macros" section was updated.	2-80
	The "JTAG" section was updated.	2-100
	In the "Data Registers (DRs)" section the IDCODE and USERCODE were changed from 32 bits to 33 bits.	2-100
	150°C was changed to 125°C in the "Thermal Characteristics" section.	2-7
	Table 2-8 • Package Thermal Characteristics was updated to include the 1152 CCGA. Values in the table were updated.	2-7
	A note was added to the "FIFO" section.	2-90
	Table 2-7 • Different Components Contributing to the Total Power Consumption in RTAX-S/SL Devices was updated.	2-4
	Table 2-17 was updated.	2-20
	All Timing Characteristic tables from Table 2-22 to Table 2-84 were updated.	2-25 to 2-81
	In the "Actel MIL-STD-883 Class B Product Flow" table, #3 for the 883 Method was updated. A note was also added to the table.	i-iv
	In the "Actel Extended Flow" table, #5 for the Method column was updated. The notes were also added to the table.	i-iv
	In the "Pin Descriptions" section, the descriptions for the "HCLKA/B/C/D Dedicated (Hardwired) Clocks A, B, C, and D" and "CLKE/F/G/H Global Clocks E, F, G, and H" were updated.	2-11
	A footnote was added to the "PRA/B/C/D Probes A, B, C, and D", "TCK2 Test Clock", "TDI2 Test Data Input", "TDO2 Test Data Output", and "TDO2 Test Data Output" descriptions.	2-12
	The "1152-Pin CCGA/LGA" section is new.	3-45
Advanced v0.4	LET_{TH} values for SEU and SEL updated under "Designed for Space".	i-i
	"Ordering Information" was updated/ The "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix"tables are new and the "Device Resources" was updated.	i-ii
	Sections "Actel MIL-STD-883 Class B Product Flow" and "Actel Extended Flow" are new.	i-iv, i-v
	"General Description" was updated.	1-1
	Table 2-7 • Different Components Contributing to the Total Power Consumption in RTAX-S/SL Devices was updated.	2-4
	The"Thermal Characteristics" section was updated.	2-7
	Figure 2-4 • Timing Model, the "Hardwired Clock"section and the "Routed Clock1" section were updated.	2-10

Previous version	Changes in current version (v5.4)	Page
Advanced v.04 (continued)	The "Introduction" section under "User I/Os" was updated to give details regarding V_{REF} usage.	2-12
	The "Simultaneous Switching Outputs (SSO)" section under "User I/Os" was updated.	2-14
	"Using DDR (Double Data Rate)" is new.	2-17
	Table 2-18 was updated.	2-22
	All Timing Characteristic Tables were updated.	2-25 to 2-99
	"Introduction" was updated.	2-66
	The "SEU Hardened D Flip-Flop (DFF)" section was moved under "R-Cell" and updated.	2-67
	The "Global Resource Distribution" section is new.	2-78
	The "Enhancing SEU Performance" section is new.	2-83
	Figure 2-49 and Figure 2-50 were updated.	2-84
	Figure 2-57 and Figure 2-58 were updated.	2-95
	The "Charge Pump Bypass" section is new.	2-100
	The "TRST" section was updated.	2-100
	The "Global Set Fuse" section is new.	2-102
	The "208-Pin CQFP" for both the RTAX250S and RTAX1000S were added.	3-1
	The "352-Pin CQFP" pin tables for both the RTAX1000S and RTAX2000S were updated.	3-8
	The "624-Pin CCGA/LGA" pin tables for both the RTAX1000S and RTAX2000S were updated.	3-26
Advanced v0.3	The "Designed for Space" section was updated.	i-i
	A new device, the RTAX250S, was added to the "Designed for Space", "Ordering Information", "Temperature Grade Offerings" and "Device Resources" sections.	i to iii
	2.5V GTL+ support across full military range was removed.	n/a
	Table 1-1 • Number of Core Tiles per Device was updated.	1-4
	Table 2-4 • RTAX-S Standby Current and Table 2-6 • Default Cload / VCCI were updated.	2-4
	Table 2-7 • Different Components Contributing to the Total Power Consumption in RTAX-S/SL Devices was updated.	2-4
	Table 2-13 • Legal I/O Usage Matrix was updated.	2-15
	Table 2-17 • I/O Macros for Voltage-Referenced I/O Standards	2-20
Advanced v0.2	In the "352-Pin CQFP" for the RTAX1000S, pin 80 has been changed from VCCI to VCCIB6.	3-14
	In the "208 CQFP" and "352-Pin CQFP", the NC (V_{PP}) was changed to NC for all pins.	3-2 to 3-14
Advanced v0.1	The 352-Pin CQFP for the RTAX1000S is new.	3-10
	Pins 14 and 32 have been changed from VCCA to VCCI for the RTAX2000S in the "352-Pin CQFP".	3-10
	The "624-Pin CCGA/LGA" for the RTAX1000S is new.	3-39

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In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

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Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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